The Hardware Book (WinHelp16)

WinHelp Edition
Hardware Book

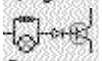
Welcome to the Hardware Book. Your electronic reference guide.
Created and maintained by Joakim Ogren.
This is the WinHelp version for Windows.
You'll find the online version at http://www.blackdown.org/~hwb/hwb.html.
Current version 0.9 Beta.
Converted from HTML 1997-01-20.

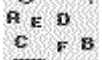

Connectors — Pinouts for connectors, buses etc.

Connectors Top 10 — Too many? These are the most common.


Cables — How to build serial cables and many other cables.

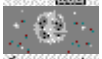

Adapters — How to build adapters.


Circuits — Coming soon.



Misc — Misc information (active filters etc).


Tables — Coming soon.


WWW Links — Links to other electronic resources.


Download — Download a WinHelp or HTML version for offline viewing.

HwB-News — Subscribe to the HwB Newsletter! Info about updates etc.

Wanted — Information I'm currently looking for.


About — Who did this? And why?

This is the URL for the WWW page:
http://www.blackdown.org/~hwb/hwb.html
Open this address in your WWW browser.

Connector Menu

What does the the information that is listed for each connector mean? See the tutorial.

Buses:

- ISA UPDATED - (Technical) NEW
- EISA UPDATED - (Technical) NEW
- PCI UPDATED - (Technical) NEW
- VESA LocalBus (VLB) UPDATED - (Technical) NEW
- CompactPCI NEW - (Technical) NEW
- IndustrialPCI NEW
- SmallPCI NEW
- Miniature Card NEW - (Technical) NEW
- Zorro II
- Zorro II/III
- CPU-port (A1200)
- Ramex (A1000)
- Video Expansion (Amiga)
- CD32 Expansion
- CardBus NEW
- PC Card NEW
- PC Card ATA NEW
- PCMCIA NEW
- CompactFlash NEW
- C-bus II NEW
- SSFDC NEW
- PC-104 NEW

In/Out:

- RS-232 UPDATED
- Serial (PC 9)
- Serial (PC 25) UPDATED
- Serial (Amiga 1000) NEW
- Serial (Amiga) NEW
- Serial (MSX) NEW
- DEC Dual RS-232 NEW

- Macintosh RS-422 NEW
- C64 RS232 User Port NEW
- Parallel (PC)
- Parallel (Amiga)
- Parallel (Amiga 1000) NEW
- ECP Parallel NEW - (Technical) NEW
- Centronics Printer
- MSX Parallel NEW
- GeekPort NEW
- C64 Serial I/O

Video:

- VGA (VESA DDC) NEW
- VGA (15) NEW
- VGA (9)
- CGA
- EGA
- PGA
- MDA (Hercules)
- VGA Feature
- Macintosh Video NEW
- Amiga Video
- RF Monitor (Amiga 1000) NEW
- CDTV Video Slot
- PlayStation A/V NEW
- Commodore 1084 & 1084S (Analog)
- Commodore 1084 & 1084S (Digital)
- Commodore 1084d & 1084dS
- Atari Jaguar A/V NEW
- SNES Video NEW
- Sun Video NEW
- ZX Spectrum 128 RGB NEW
- 3b1-7300 Video NEW
- CM-8/CoCo RGB NEW
- AT&T 53D410 NEW
- AT&T 6300 Taxan Monitor NEW
- AT&T PC6300 NEW
- Vic 20 Video NEW
- C64 Audio/Video
- C65 Video NEW
- C128 RGBI NEW
- C128/C64C Video NEW
- CBM 1902A NEW

Joysticks/Mouses:

- PC Gameport NEW
- PC Gameport+MIDI NEW

- Amiga Mouse/Joy NEW
- MSX Joystick NEW
- SGI Mouse (Model 021-0004-002) NEW
- Atari Enhanced Joystick NEW
- Atari 2600 Joystick NEW
- Atari 6200 Joystick NEW
- Atari 7800 Joystick NEW

Keyboards:

- Keyboard (5 PC)
- Keyboard (6 PC)
- Keyboard (XT)
- Keyboard (5 Amiga)
- Keyboard (6 Amiga)
- Keyboard (Amiga CD32) NEW
- AT&T 6300 Keyboard NEW

Diskdrives:

- Internal Diskdrive
- External Diskdrive (Amiga) NEW
- MSX External Diskdrive NEW

Harddrives:

- SCSI Internal
- SCSI Internal Differential NEW
- SCSI External Centronics 50
- SCSI External (Future Domain)
- SCSI External (Amiga/Mac)
- IDE Internal NEW
- ATA Internal NEW
- ATA (44) Internal NEW
- ESDI
- ST506/412
- Paravision SX-1 External IDE NEW

Misc data storage:

- C64 Cassette NEW
- CoCo Cassette NEW
- MSX Cassette NEW

Memories:

- 30 pin SIMM NEW
- 72 pin SIMM NEW
- 72 pin ECC SIMM NEW
- 72 pin SO DIMM NEW
- 144 pin SO DIMM NEW
- 168 pin DRAM DIMM (Unbuffered) NEW
- 168 pin SDRAM DIMM (Unbuffered) NEW
- CDTV Memory Card

- SmartCard AFNOR NEW
- SmartCard ISO 7816-2 NEW
- SmartCard ISO NEW

Home audio/video:

- SCART
- S-Video
- DIN Audio NEW

PC motherboards:

- Turbo LED
- AT Backup Battery
- AT LED/Keylock
- 5.25" Power
- 3.5" Power
- MotherboardPower
- PC-Speaker

Networking:

- Ethernet 10Base-T NEW
- AUI NEW

Cartridge/Expansion:

- Atari 2600 Cartridge NEW
- Atari 5200 Cartridge NEW
- Atari 5200 Expansion NEW
- Atari 7800 Cartridge NEW
- Atari 7800 Expansion NEW
- GameBoy Cartridge NEW
- MSX Expansion NEW
- Vic 20 Memory Expansion NEW
- C64 Cartridge NEW
- C64 User Port NEW
- C16/+4 Expansion Bus NEW
- C16/+4 User Port NEW
- CDTV Diagnostic Slot
- CDTV Expansion Slot
- PC-Engine Cartridge NEW
- SNES Cartridge NEW
- TG-16 Cartridge NEW
- ZX Spectrum AY-3-8912 NEW
- ZX Spectrum ULA NEW

Misc:

- MIDI Out
- MIDI In
- Minuteman UPS NEW

Last updated 1997-01-19.

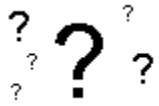
Short tutorial

Heading

First at each page there a short heading describing what the connector is.

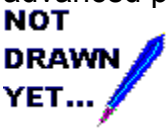
Pictures of the connectors

After that there is at each page there is one or more pictures of the connectors. Sometimes there is some question marks only. This means that I don't know what kind of connector it is or how it looks.



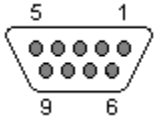
(At the computer)

There may be some pictures I haven't drawn yet. I illustrate this with the following advanced picture:

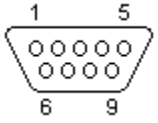


(At the computer)

Normally are one or more pictures. **These are seen from the front, and NOT the soldside. Holes (female connectors usually) are darkened.** Look at the example below. The first is a female connector and the send a male. The texts insde parentheses will tell you at which kind of the device it will look like that.



(At the videocard)



(At the monitor cable)

Texts describing the connectors

Below the pictures there is texts that describes the connectors. Including the name of the physical connector.

5 PIN DIN 180~ (DIN41524) at the computer.

Pin table

The pin table is perhaps the information you're looking for. Should be simple to read. Contains mostly the following three columns; Pin, Name & Description.

Pin	Name	Description
1	CLOCK	Key Clock
2	GND	GND
3	DATA	Key Data
4	VCC	+5 VDC
5	n/c	Not connected

Contributor & Source

All persons that helped me or sent me information about the connector will be listed here. The source of the information is perhaps a book or another site. I must admit that I'm bad at writing the source, but I'll try to fill in these in the future.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

ISA Connector

ISA

ISA=Industry Standard Architecture (not maybe a clever name, looking at all problems that exists today :-)

```
+-----------------------------------------------+
|              (component side)                 |
|                                               |
|_____________ ISA-16bit __        ISA-8bit   __|
              ||||||||||||  ||||||||||||||||||  A1(front)/B1(back)
                        C1/D1
```

A,C=Component Side

B,D=Sold Side

(At the computer)

62+36 PIN EDGE CONNECTOR at the computer.

Pin	Name	Dir	Description
A1	/I/O CH CK	←	I/O channel check; active low=parity error
A2	D7	↔	Data bit 7
A3	D6	↔	Data bit 6
A4	D5	↔	Data bit 5
A5	D4	↔	Data bit 4
A6	D3	↔	Data bit 3
A7	D2	↔	Data bit 2
A8	D1	↔	Data bit 1
A9	D0	↔	Data bit 0
A10	I/O CH RDY	NEW	I/O Channel ready, pulled low to lengthen memory cycles
A11	AEN	→	Address enable; active high when DMA controls bus
A12	A19	→	Address bit 19
A13	A18	→	Address bit 18
A14	A17	→	Address bit 17
A15	A16	→	Address bit 16
A16	A15	→	Address bit 15
A17	A14	→	Address bit 14
A18	A13	→	Address bit 13
A19	A12	NEW	Address bit 12
A20	A11	NEW	Address bit 11
A21	A10	NEW	Address bit 10
A22	A9	NEW	Address bit 9
A23	A8	NEW	Address bit 8
A24	A7	NEW	Address bit 7

A25	A6	NEW	Address bit 6
A26	A5	NEW	Address bit 5
A27	A4	NEW	Address bit 4
A28	A3	NEW	Address bit 3
A29	A2	NEW	Address bit 2
A30	A1	NEW	Address bit 1
A31	A0	NEW	Address bit 0
B1	GND		Ground
B2	RESET	NEW	Active high to reset or initialize system logic
B3	+5V		+5 VDC
B4	IRQ2	NEW	Interrupt Request 2
B5	-5VDC		-5 VDC
B6	DRQ2	NEW	DMA Request 2
B7	-12VDC		-12 VDC
B8	/CARD SLCTD	NEW	Card selected; activated by cards in XT's slot J8
B9	+12VDC		+12 VDC
B10	GND		Ground
B11	/SMEMW	NEW	System Memory Write
B12	/SMEMR	NEW	System Memory Read
B13	/IOW	NEW	I/O Write
B14	/IOR	NEW	I/O Read
B15	/DACK3	NEW	DMA Acknowledge 3
B16	DRQ3	NEW	DMA Request 3
B17	/DACK1	NEW	DMA Acknowledge 1
B18	DRQ1	NEW	DMA Request 1
B19	/REFRESH	NEW	Refresh
B20	CLOCK	NEW	System Clock (67 ns, 8-8.33 MHz, 50% duty cycle)
B21	IRQ7	NEW	Interrupt Request 7
B22	IRQ6	NEW	Interrupt Request 6
B23	IRQ5	NEW	Interrupt Request 5
B24	IRQ4	NEW	Interrupt Request 4
B25	IRQ3	NEW	Interrupt Request 3
B26	/DACK2	NEW	DMA Acknowledge 2
B27	T/C	NEW	Terminal count; pulses high when DMA term. count reached
B28	ALE	NEW	Address Latch Enable
B29	+5V		+5 VDC
B30	OSC	NEW	High-speed Clock (70 ns, 1431818 MHz, 50% duty cycle)
B31	GND		Ground
C1	SBHE	NEW	System bus high enable (data availble on SD8-15)
C2	LA23	NEW	Address bit 23
C3	LA22	NEW	Address bit 22
C4	LA21	NEW	Address bit 21
C5	LA20	NEW	Address bit 20
C6	LA18	NEW	Address bit 19
C7	LA17	NEW	Address bit 18
C8	LA16	NEW	Address bit 17
C9	/MEMR	NEW	Memory Read (Active on all memory read cycles)
C10	/MEMW	NEW	Memory Write (Active on all memory write cycles)
C11	SD08	NEW	Data bit 8
C12	SD09	NEW	Data bit 9
C13	SD10	NEW	Data bit 10
C14	SD11	NEW	Data bit 11
C15	SD12	NEW	Data bit 12
C16	SD13	NEW	Data bit 13
C17	SD14	NEW	Data bit 14

C18	SD15	NEW	Data bit 15
D1	/MEMCS16	NEW	Memory 16-bit chip select (1 wait, 16-bit memory cycle)
D2	/IOCS16	NEW	I/O 16-bit chip select (1 wait, 16-bit I/O cycle)
D3	IRQ10	NEW	Interrupt Request 10
D4	IRQ11	NEW	Interrupt Request 11
D5	IRQ12	NEW	Interrupt Request 12
D6	IRQ15	NEW	Interrupt Request 15
D7	IRQ14	NEW	Interrupt Request 14
D8	/DACK0	NEW	DMA Acknowledge 0
D9	DRQ0	NEW	DMA Request 0
D10	/DACK5	NEW	DMA Acknowledge 5
D11	DRQ5	NEW	DMA Request 5
D12	/DACK6	NEW	DMA Acknowledge 6
D13	DRQ6	NEW	DMA Request 6
D14	/DACK7	NEW	DMA Acknowledge 7
D15	DRQ7	NEW	DMA Request 7
D16	+5 V		
D17	/MASTER	NEW	Used with DRQ to gain control of system
D18	GND		Ground

Note: Direction is Motherboard relative ISA-Cards.

Contributor: Joakim Ogren

Source:IBM PC/AT Technical Reference, pages 1-25 through 1-37

Please send any comments to Joakim Ogren.

ISA (Technical)

This file is designed to give a basic overview of the bus found in most IBM clone computers, often referred to as the XT or AT bus. The AT version of the bus is upwardly compatible, which means that cards designed to work on an XT bus will work on an AT bus. This bus was produced for many years without any formal standard. In recent years, a more formal standard called the ISA bus (Industry Standard Architecture) has been created, with an extension called the EISA (Extended ISA) bus also now as a standard. The EISA bus extensions will not be detailed here.

This file is not intended to be a thorough coverage of the standard. It is for informational purposes only, and is intended to give designers and hobbyists sufficient information to design their own XT and AT compatible cards.

Signal Descriptions:

+5, -5, +12, -12

Power supplies. -5 is often not implimented.

AEN

Address Enable. This is asserted when a DMAC has control of the bus. This prevents an I/O device from responding to the I/O command lines during a DMA transfer. When AEN is active, the DMA Controller has control of the address bus as the memory and I/O read/write command lines.

BALE

Bus Address Latch Enable. The address bus is latched on the rising edge of this signal. The address on the SA bus is valid from the falling edge of BALE to the end of the bus cycle. Memory devices should latch the LA bus on the falling edge of BALE. Some references refer to this signal as Buffered Address Latch Enable, or just Address Latch Enable (ALE). The Buffered-Address Latch Enable is used to latch SA0-19 on the falling edge. This signal is forced high during DMA cycles.

BCLK

Bus Clock, 33% Duty Cycle. Frequency Varies. 4.77 to 8 MHz typical. 8.3 MHz is specified as the maximum, but many systems allow this clock to be set to 12 MHz and higher.

SD0-SD16

System Data lines, or Standard Data Lines. They are bidirectional and tri-state. These 16 lines provide for data transfer between the processor, memory and I/O devices.

DACKx

DMA Acknowledge. The active-low DMA Acknowledge 0 to 3 and 5 to 7 are the corresponding acknowledge signals for DRQ 0-3, 5-7.

DRQx

DMA Request. These signals are asynchronous channel requests used by I/O channel devices to gain DMA service. DMA request channels 0-3 are for 8-bit data transfer. DAM request channels 5-7 are for 16-bit data transfer. DMA request channel 4 is used internally on the system board. DMA requests should be held high until the corresponding DACK line goes active. DMA requests are serviced in the following priority sequence:
High: DRQ 0, 1, 2, 3, 5, 6, 7 Lowest

IOCS16

I/O size 16. Generated by a 16 bit slave when addressed by a bus master. The active-low I/O Chip Select 16 indicates that the current transfer is a 1 wait state, 16 bit I/O cycle. Open Collector.

I/O CH CK

Channel Check. A low signal generates an NMI. The NMI signal can be masked on a PC, externally to the processor (of course). Bit 7 of port 70(hex) (enable NMI interrupts) and bit 3 of port 61 (hex) (recognition of channel check) must both be set to zero for an NMI to reach the cpu. The I/O Channel Check is an active-low signal which indicates that a parity error exists in a device on the I/O channel.

I/O CH RDY

Channel Ready. Setting this low prevents the default ready timer from timing out. The slave device may then set it high again when it is ready to end the bus cycle. Holding this line low for too long can prevent RAM refresh cycles on some systems. This signal is called IOCHRDY (I/O Channel Ready) by some references. CHRDY and NOWS should not be used simultaneously. This may cause problems with some bus controllers. This signal is pulled low by a memory or I/O device to lengthen memory or I/O read/write cycles. It should only be held low for a maimum of 2.5 microseconds.

IOR

The I/O Read is an active-low signal which instrucs the I/O device to drive its data onto the data bus, SD0-SD15.

IOW

The I/O Write is an active-low signal which instructs the I/O device to read data from the data bus, SD0-SD15.

IRQx

Interrupt Request. IRQ2 has the highest priority. IRQ 10-14 are only available on AT machines, and are higher priority than IRQ 3-7. The Interrupt Request signals which indicate I/O service attention. They are prioritized in the following sequence: Highest IRQ 9(2),10,11,12,14,3,4,5,6,7

LAxx

Latchable Address lines. Combine with the lower address lines to form a 24 bit address space (16 MB) These unlatched address signals give the system up to 16 MB of address ability. The are valid when "BALE" is high.

MASTER

16 bit bus master. Generated by the ISA bus master when initiating a bus cycle. This active-low signal is used in conjuction with a DRQ line by a processor on the I/O channel to gain control of the system. The I/O processor first issues a DRQ, and upon recieving the corresponding DACK, the I/O processor may assert MASTER, which will allow it to control the system address, data and control lines. This signal should not be assrted for more than 15 microseconds, or system memory may be corrupted du to the lack of memory refresh activity.

MEMCS16

The active-low Memory Chip Select 16 indicates that the current data transfer is a 1 wait state, 16 bit data memory cycle.

MEMR

The Memory Read is an active-low signal which instructs memory devices to drive data onto the data bus SD0-SD15. This signal is active on all memory read cycles.

MEMW

The Memory Write is an active-low signal which instructs memory devices to store data present on the data bus SD0-SD15. This signal is active on all memory write cycles.

NOWS

No Wait State. Used to shorten the number of wait states generated by the default ready timer. This causes the bus cycle to end more quickly, since wait states will not be inserted. Most systems will ignore NOWS if CHRDY is active (low). However, this may cause problems with some bus controllers, and both signals should not be active simultaneously.

OSC

Oscillator, 14.31818 MHz, 50% Duty Cycle. Frequency varies. This was originally divided by 3 to provide the 4.77 MHz cpu clock of early PCs, and divided by 12 to produce the 1.19 MHz system clock. Some references have placed this signal as low as 1 MHz (possibly referencing the system clock).

REFRESH

Refresh. Generated when the refresh logic is bus master. This active-low signal is used to indicate a memory refresh cycle is in progress.

RESET

This signal goes low when the machine is powered up. Driving it low will force a system reset. This signal goes high to reset the system during powerup, low line-voltage or

hardware reset. ??????????????

SA0-SA19

System Address Lines, tri-state. The System Address lines run from bit 0 to bit 19. They are latched on to the falling edge of "BALE".

SBHE

System Bus High Enable, tristate. Indicates a 16 bit data transfer. The System Bus High Enable indicates high byte transfer is occuring on the data bus SD8-SD15.

SMEMR

System Memory Read Command line. Indicates a memory read in the lower 1 MB area. This System Memory Read is an active-low signal which instructs memory devices to drive data onto the data bus SD0-SD15. This signal is active only when the memory address is within the lowest 1MB of memory address space.

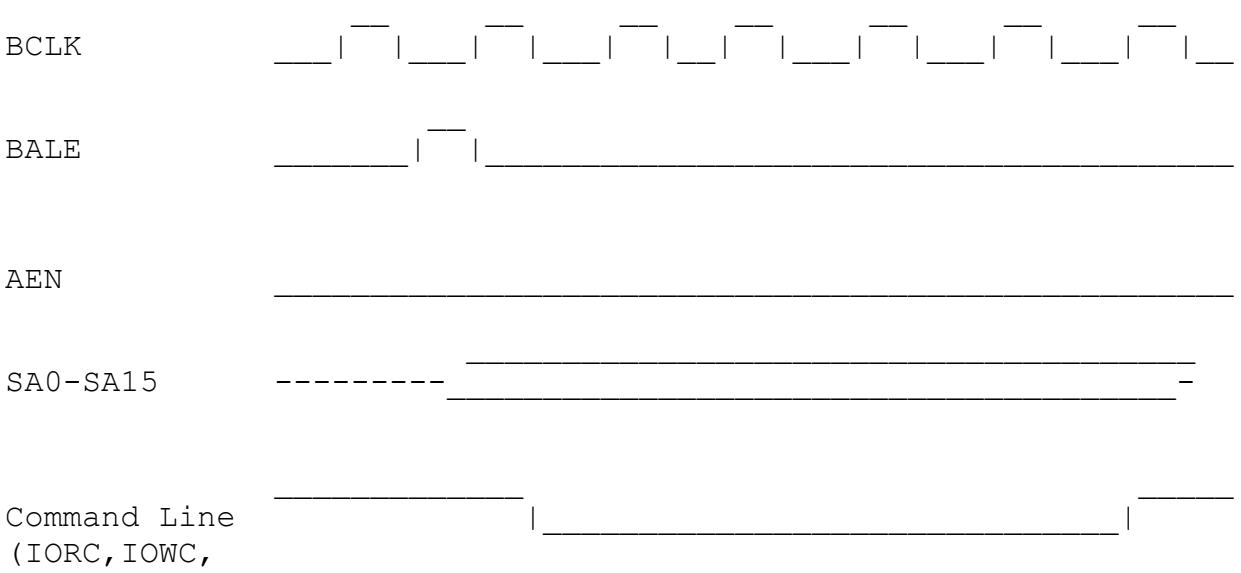
SMEMW

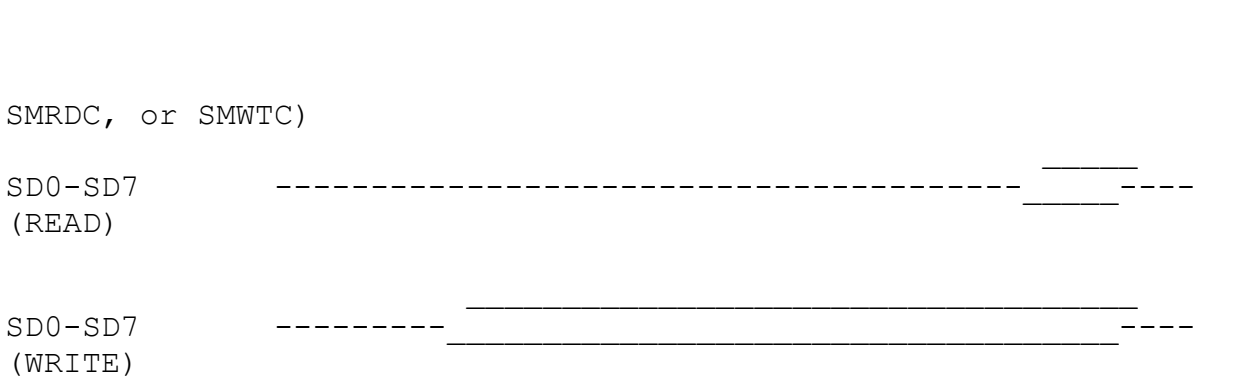
System Memory Write Commmand line. Indicates a memory write in the lower 1 MB area. The System Memory Write is an active-low signal which instructs memory devices to store data preset on the data bus SD0-SD15. This signal is active only when the memory address is within the lowest 1MB of memory address space.

T/C

Terminal Count. Notifies the cpu that that the last DMA data transfer operation is complete. Terminal Count provides a pulse when the terminal count for any DMA channel is reached.

8 Bit Memory or I/O Transfer Timing Diagram (4 wait states shown)





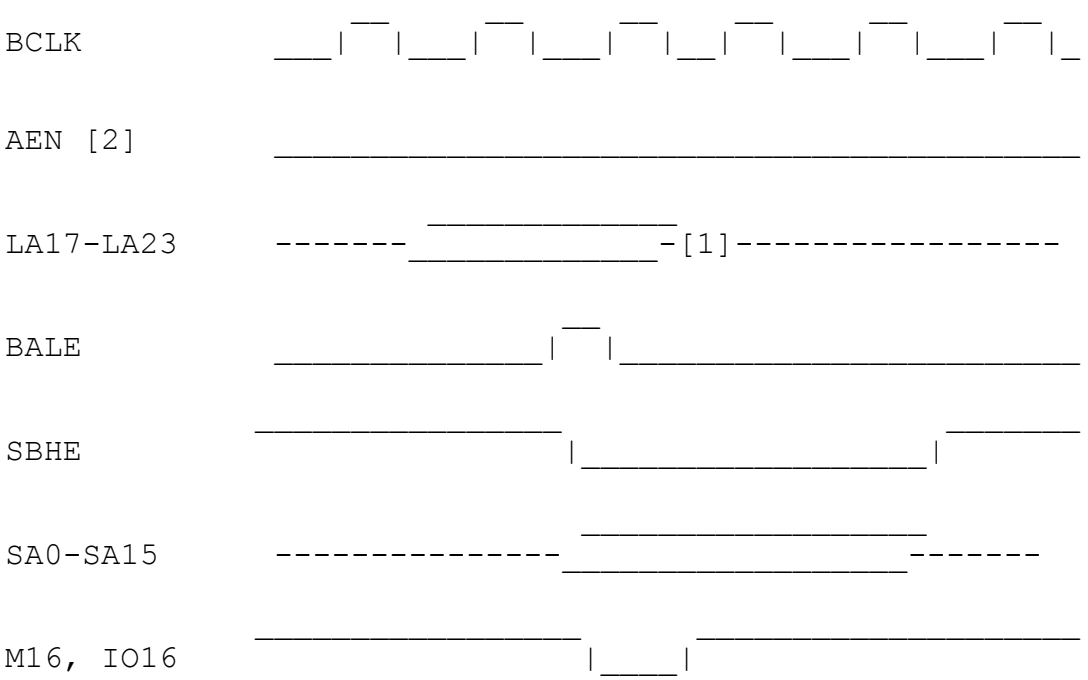
BALE is placed high, and the address is latched on the SA bus. The slave device may safely sample the address during the falling edge of BALE, and the address on the SA bus remains valid until the end of the transfer cycle. Note that AEN remains low throughout the entire transfer cycle.

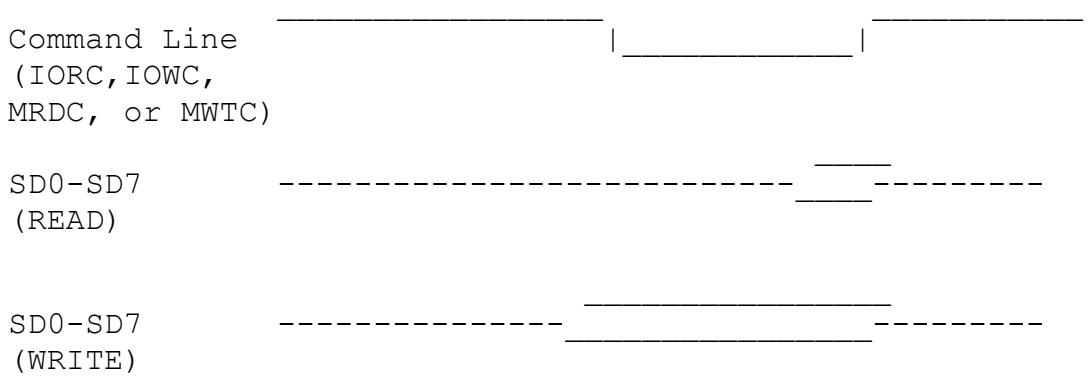
The command line is then pulled low (IORC or IOWC for I/O commands, SMRDSC or SMWTC for memory commands, read and write respectively). For write operations, the data remaines on the SD bus for the remainder of the transfer cycle. For read operations, the data must be valid on the falling edge of the last cycle.

NOWS is sampled at the midpoint of each wait cycle. If it is low, the transfer cycle terminates without further wait states. CHRDY is sampled during the first half of the clock cycle. If it is low, further wait cycles will be inserted.

The default for 8 bit transfers is 4 wait states. Some computers allow the number of default wait states to be changed.

16 Bit Memory or I/O Transfer Timing Diagram (1 wait state shown)





[1] The portion of the address on the LA bus for the NEXT cycle may now be placed on the bus. This is used so that cards may begin decoding the address early. Address pipelining must be active.

[2] AEN remains low throughout the entire transfer cycle, indicating that a normal (non-DMA) transfer is occuring.

16 bit transfers follow the same basic timing as 8 bit transfers. The LA bus is not latched, and a valid address may appear on the LA bus prior to the beginning of the transfer cycle. Unlike the SA bus, the LA bus is not latched, and is not valid for the entire transfer cycle.

The default for 16 bit transfers is 1 wait state. This may be shortened or lengthened in the same manner as 8 bit transfers, via NOWS and CHRDY.

SMRDC/SMWTC follow the same timing as MRDC/MWTC respectively when the address is within the lower 1 MB. If the address is not within the lower 1 MB boundary, SMRDC/SMWTC will remain high during the entire cycle.

SBHE must be pulled low to activate the upper portion of the bus (LA, SD8-15, etc). To transfer 16 bits (instead of 8), M16 or IO16 must be pulled low by the slave device (if it is a memory or I/O device, respectively).

Note: Only the first 10 address lines are decoded for I/O operations.

Port (hex)	**Port Assignments**
000-00F	DMA #1
020-021	PIC #1
040-043	PIT
060-063	Keyboard Controller
070-071	Real Time Clock
080-083	DMA Page Register
0A0-0AF	PIC #2
0C0-0CF	DMA #2
0E0-0EF	reserved
0F0-0FF	coprocessor
100-1FF	AVAILABLE
200-20F	Game Adapter
210-217	reserved
220-26F	AVAILABLE
278-27F	Parallel Interface #2

2B0-2DF	EGA
2F8-2FF	COM2
300-31F	Prototype Adapter
320-32F	AVAILABLE
378-37F	Parallel Interface #1
380-38F	SDLC Adapter
3A0-3AF	reserved
3B0-3BF	Monochome Adapter/Parallel Interface
3C0-3CF	EGA

DMA Read and Write

The ISA bus uses two DMA controllers (DMAC) cascaded together. The slave DMAC connects to the master DMAC via DMA channel 4 (channel 0 on the master DMAC). The slave therefore gains control of the bus through the master DMAC. On the ISA bus, the DMAC is programmed to use fixed priority (channel 0 always has the highest priority), which means that channel 0-4 from the slave have the highest priority (since they connect to the master channel 0), followed by channels 5-7 (which are channel 1-3 on the master).

The DMAC can be programmed for read transfers (data is read from memory and written to the I/O device), write transfers (data is read from the I/O device and written to memory), or verify transfers (neither a read or a write - this was used by DMA CH0 for DRAM refresh on early PCs).

Before a DMA transfer can take place, the DMA Controller (DMAC) must be programmed. This is done by writing the start address and the number of bytes to transfer (called the transfer count) and the direction of the transfer to the DMAC. After the DMAC has been programmed, the device may activate the appropriate DMA request (DRQx) line.

Slave DMA Controller

I/O	**Port**
0000	DMA CH0 Memory Address Register Contains the lower 16 bits of the memory address, written as two consecutive bytes.
0001	DMA CH0 Transfer Count Contains the lower 16 bits of the transfer count, written as two consecutive bytes.
0002	DMA CH1 Memory Address Register
0003	DMA CH1 Transfer Count
0004	DMA CH2 Memory Address Register
0005	DMA CH2 Transfer Count
0006	DMA CH3 Memory Address Register
0007	DMA CH3 Transfer Count
0008	DMAC Status/Control Register Status (I/O read) bits 0-3: Terminal Count, CH 0-3 - bits 4-7: Request CH0-3 Control (write) - bit 0: Mem to mem enable (1 = enabled) - bit 1: ch0 address hold enable (1 = enabled) - bit 2: controller disable (1 = disabled)

- bit 3: timing (0 = normal, 1 = compressed)
- bit 4: priority (0 = fixed, 1 = rotating)
- bit 5: write selection (0 = late, 1 = extended)
- bit 6: DRQx sense asserted (0 = high, 1 = low)
- bit 7: DAKn sense asserted (0 = low, 1 = high)

0009 Software DRQn Request
- bits 0-1: channel select (CH0-3)
- bit 2: request bit (0 = reset, 1 = set)

000A DMA mask register
- bits 0-1: channel select (CH0-3)
- bit 2: mask bit (0 = reset, 1 = set)

000B DMA Mode Register
- bits 0-1: channel select (CH0-3)
- bits 2-3: 00 = verify transfer, 01 = write transfer, 10 = read transfer, 11 = reserved
- bit 4: Auto init (0 = disabled, 1 = enabled)
- bit 5: Address (0 = increment, 1 = decrement)
- bits 6-7: 00 = demand transfer mode, 01 = single transfer mode, 10 = block transfer mode, 11 = cascade mode

000C DMA Clear Byte Pointer
Writing to this causes the DMAC to clear the pointer used to keep track of 16 bit data transfers into and out of the DMAC for hi/low byte sequencing.

000D DMA Master Clear (Hardware Reset)

000E DMA Reset Mask Register - clears the mask register

000F DMA Mask Register
- bits 0-3: mask bits for CH0-3 (0 = not masked, 1 = masked)

0081 DMA CH2 Page Register (address bits A16-A23)

0082 DMA CH3 Page Register

0083 DMA CH1 Page Register

0087 DMA CH0 Page Register

0089 DMA CH6 Page Register

008A DMA CH7 Page Register

008B DMA CH5 Page Register

Master DMA Controller

I/O **Port**

00C0 DMA CH4 Memory Address Register
Contains the lower 16 bits of the memory address, written as two consecutive bytes.

00C2 DMA CH4 Transfer Count
Contains the lower 16 bits of the transfer count, written as two consecutive bytes.

00C4 DMA CH5 Memory Address Register

00C6 DMA CH5 Transfer Count

00C8 DMA CH6 Memory Address Register

00CA DMA CH6 Transfer Count

00CC DMA CH7 Memory Address Register

00CE DMA CH7 Transfer Count

00D0 DMAC Status/Control Register
Status (I/O read) bits 0-3: Terminal Count, CH

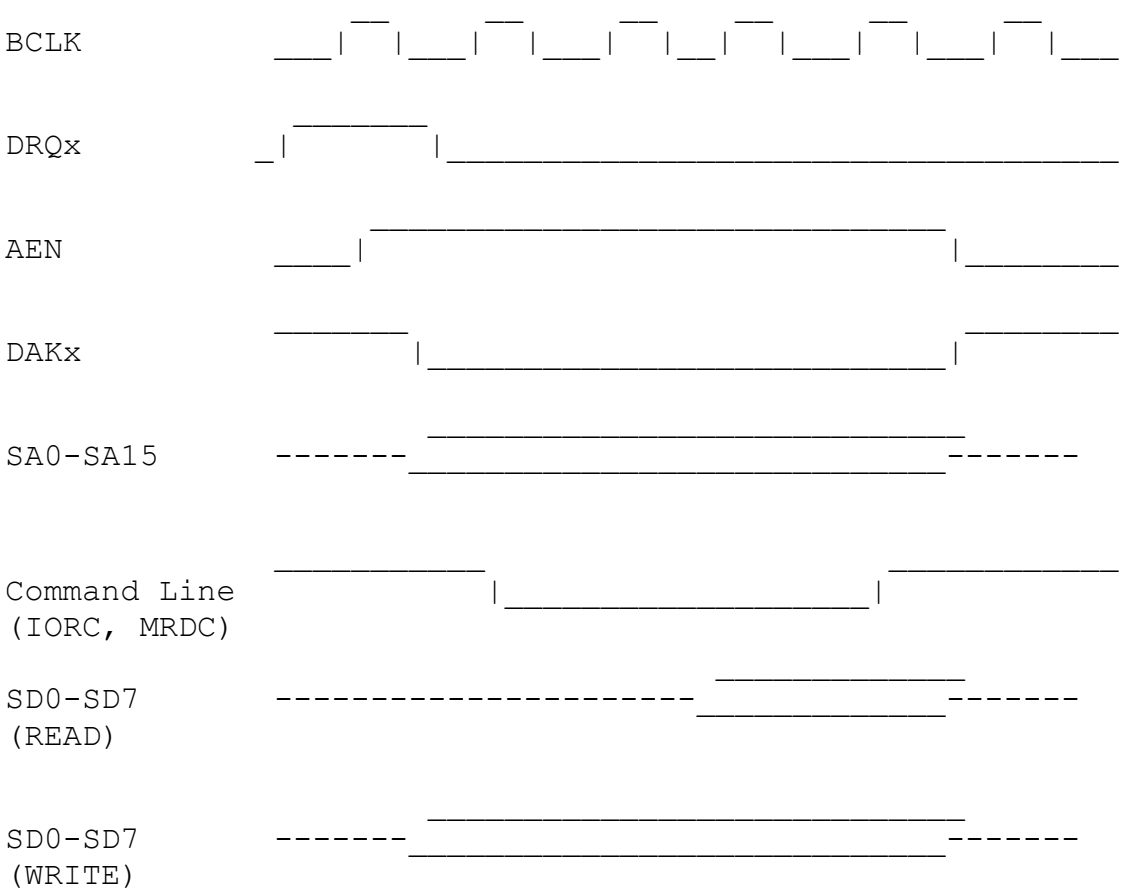
	4-7 - bits 4-7: Request CH4-7 Control (write)- bit 0: Mem to mem enable (1 = enabled) - bit 1: ch0 address hold enable (1 = enabled) - bit 2: controller disable (1 = disabled) - bit 3: timing (0 = normal, 1 = compressed) - bit 4: priority (0 = fixed, 1 = rotating) - bit 5: write selection (0 = late, 1 = extended) - bit 6: DRQx sense asserted (0 = high, 1 = low) - bit 7: DAKn sense asserted (0 = low, 1 = high)
00D2	Software DRQn Request - bits 0-1: channel select (CH4-7) - bit 2: request bit (0 = reset, 1 = set)
00D4	DMA mask register - bits 0-1: channel select (CH4-7) - bit 2: mask bit (0 = reset, 1 = set)
00D6	DMA Mode Register - bits 0-1: channel select (CH4-7) - bits 2-3: 00 = verify transfer, 01 = write transfer, 10 = read transfer, 11 = reserved - bit 4: Auto init (0 = disabled, 1 = enabled) - bit 5: Address (0 = increment, 1 = decrement) - bits 6-7: 00 = demand transfer mode, 01 = single transfer mode, 10 = block transfer mode, 11 = cascade mode
00D8	DMA Clear Byte Pointer Writing to this causes the DMAC to clear the pointer used to keep track of 16 bit data transfers into and out of the DMAC for hi/low byte sequencing.
00DA	DMA Master Clear (Hardware Reset)
00DC	DMA Reset Mask Register - clears the mask register
00DE	DMA Mask Register - bits 0-3: mask bits for CH4-7 (0 = not masked, 1 = masked)

Single Transfer Mode

The DMAC is programmed for transfer. The DMA device requests a transfer by driving the appropriate DRQ line high. The DMAC responds by asserting AEN and acknowledges the DMA request through the appropriate DAK line. The I/O and memory command lines are also asserted. When the DMA device sees the DAK signal, it drops the DRQ line.

The DMAC places the memory address on the SA bus (at the same time as the command lines are asserted), and the device either reads from or writes to memory, depending on the type of transfer. The transfer count is incrimented, and the address incrimented/decrimented. DAK is de-asserted. The cpu now once again has control of the bus, and continues execution until the I/O device is once again ready for transfer. The DMA device repeats the procedure, driving DRQ high and waiting for DAK, then transferring data. This continues for a number of cycles equal to the transfer count. When this has been completed, the DMAC signals the cpu that the DMA transfer is

complete via the TC (terminal count) signal.



Block Transfer Mode

The DMAC is programmed for transfer. The device attempting DMA transfer drives the appropriate DRQ line high. The motherboard responds by driving AEN high and DAK low. This indicates that the DMA device is now the bus master. In response to the DAK signal, the DMA device drops DRQ. The DMAC places the address for DMA transfer on the address bus. Both the memory and I/O command lines are asserted (since DMA involves both an I/O and a memory device). AEN prevents I/O devices from responding to the I/O command lines, which would not result in proper operation since the I/O lines are active, but a memory address is on the address bus. The data transfer is now done (memory read or write), and the DMAC incriments/decriments the address and begins another cycle. This continues for a number of cycles equal to the DMAC transfer count. When this has been completed, the terminal count signal (TC) is generated by the DMAC to inform the cpu that the DMA transfer has been completed.

Note: Block transfer must be used carefully. The bus cannot be used for other things (like RAM refresh) while block mode transfers are being done.

Demand Transfer Mode

The DMAC is programmed for transfer. The device attempting DMA transfer drives the appropriate DRQ line high. The motherboard responds by driving AEN high and DAK low. This indicates that the DMA device is now the bus master. Unlike single transfer and block transfer, the DMA device does not drop DRQ in response to DAK. The DMA device transfers data in the same manner as for block transfers. The DMAC will continue to generate DMA cycles as long as the I/O device asserts DRQ. When the I/O device is unable to continue the transfer (if it no longer had data ready to transfer, for example), it drops DRQ and the cpu once again has control of the bus. Control is returned to the DMAC by once again asserting DRQ. This continues until the terminal count has been reached, and the TC signal informs the cpu that the transfer has been completed.

Interrupts on the ISA bus

Name	Interrupt
NMI	2
IRQ0	8
IRQ1	9
IRQ2	A
IRQ3	B
IRQ4	C
IRQ5	D
IRQ6	E
IRQ7	F
IRQ8	F
IRQ9	F
IRQ10	F
IRQ11	F
IRQ12	F
IRQ13	F
IRQ14	F
IRQ15	F

IRQ0,1,2,8, and 13 are not available on the ISA bus.

Contributor: Joakim Ogren, Niklas Edmundsson, Mark Sokos

Sources:Mark Sokos ISA page
Sources:"ISA System Architecture, 3rd Edition" by Tom Shanley and Don Anderson ISBN 0-201-40996-8
Sources:"Eisa System Architecture, 2nd Edition" by Tom Shanley and Don Anderson ISBN 0-201-40995-X
Sources:"Microcomputer Busses" by R.M. Cram ISBN 0-12-196155-9
Sources:ZIDA 80486 Mother Board User's Manual, OPTi 486, 82C495sx

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http://www.gl.umbc.edu/~msokos1/isa.txt
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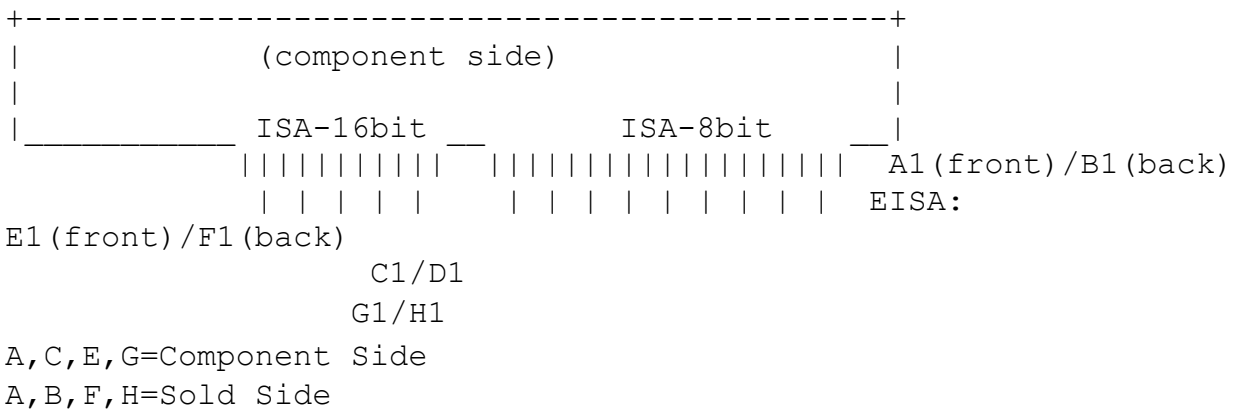
EISA Connector

NEW
NEW
NEW

EISA

EISA=Extended Industry Standard Architecture.
Developed by Compaq, AST, Zenith, Tandy...



NEW (At the computer)
62+38 PIN EDGE CONNECTOR at the computer.

Pin	Name	Description
E1	CMD#	Command Phase
E2	START#	Start Phase
E3	EXRDY	EISA Ready
E4	EX32#	EISA Slave Size 32
E5	GND	Ground
E6	KEY	Access Key
E7	EX16#	EISA Slave Size 16
E8	SLBURST#	Slave Burst
E9	MSBURST#	Master Burst
E10	W/R#	Write/Read
E11	GND	Ground
E12	RES	Reserved
E13	RES	Reserved
E14	RES	Reserved
E15	GND	Ground
E16	KEY	Access Key
E17	BE1#	Byte Enable 1
E18	LA31#	Latchable Addressline 31
E19	GND	Ground
E20	LA30#	Latchable Addressline 30
E21	LA28#	Latchable Addressline 28
E22	LA27#	Latchable Addressline 27
E23	LA25#	Latchable Addressline 25
E24	GND	Ground
E25	KEY	Access Key
E26	LA15	Latchable Addressline 15
E27	LA13	Latchable Addressline 13
E28	LA12	Latchable Addressline 12
E29	LA11	Latchable Addressline 11

E30	GND	Ground
E31	LA9	Latchable Addressline 9
F1	GND	Ground
F2	+5V	+5 VDC
F3	+5V	+5 VDC
F4	---	
F5	---	
F6	KEY	Access Key
F7	---	
F8	---	
F9	+12V	+12 VDC
F10	M/IO#	Memory/Input-Output
F11	LOCK#	Lock bus
F12	RES	Reserved
F13	GND	Ground
F14	RES	Reserved
F15	BE3#	Byte Enable 3
F16	KEY	Access Key
F17	BE2#	Byte Enable 2
F18	BE0#	Byte Enable 0
F19	GND	Ground
F20	+5V	+5 VDC
F21	LA29#	Latchable Addressline 29
F22	GND	Ground
F23	LA26#	Latchable Addressline 26
F24	LA24#	Latchable Addressline 24
F25	KEY	Access Key
F26	LA16	Latchable Addressline 16
F27	LA14	Latchable Addressline 14
F28	+5V	+5 VDC
F29	+5V	+5 VDC
F30	GND	Ground
F31	LA10	Latchable Addressline 10
G1	LA7	Latchable Addressline 7
G2	GND	Ground
G3	LA4	Latchable Addressline 4
G4	LA3	Latchable Addressline 3
G5	GND	Ground
G6	KEY	Access Key
G7	D17	Data 17
G8	D19	Data 19
G9	D20	Data 20
G10	D22	Data 22
G11	GND	Ground
G12	D25	Data 25
G13	D26	Data 26
G14	D28	Data 28
G15	KEY	Access Key
G16	GND	Ground
G17	D30	Data 30
G18	D31	Data 31
G19	MREQx	Master Request
H1	LA8	Latchable Addressline 8

H2	LA6	Latchable Addressline 6
H3	LA5	Latchable Addressline 5
H4	+5V	+5 VDC
H5	LA2	Latchable Addressline 2
H6	KEY	Access Key
H7	D16	Data 16
H8	D18	Data 18
H9	GND	Ground
H10	D21	Data 21
H11	D23	Data 23
H12	D24	Data 24
H13	GND	Ground
H14	D27	Data 27
H15	KEY	Access Key
H16	D29	Data 29
H17	+5V	+5 VDC
H18	+5V	+5 VDC
H19	MAKx	Master Acknowledge

Contributor: Joakim Ogren, Mark Sokos

Sources:Mark Sokos EISA page

Sources:"Eisa System Architecture, 2nd Edition" by Tom Shanley and Don Anderson, ISBN 0-201-40995-X

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.gl.umbc.edu/~msokos1/eisa.txt
Open this address in your WWW browser.

EISA (Technical)

This section is currently based soly on the work by Mark Sokos.

This file is intended to provide a basic functional overview of the EISA Bus, so that hobbyists and ametuers can design their own EISA compatible cards.

It is not intended to provide complete coverage of the EISA standard.

EISA is an acronym for Extended Industry Standard Architecture. It is an extension of the ISA architecture, which is a standardized version of the bus originally developed by IBM for their PC computers. EISA is upwardly compatible, which means that cards originally designed for the 8 bit IBM bus (often referred to as the XT bus) and cards designed for the 16 bit bus (referred to as the AT bus, and also as the ISA bus), will work in an EISA slot. EISA specific cards will not work in an AT or an XT slot.

The EISA connector uses multiple rows of connectors. The upper row is the same as a regular ISA slot, and the lower row contains the EISA extension. The slot is keyed so that ISA cards cannot be inserted to the point where they connet with the EISA signals.

Signal Descriptions

+5, -5, +12, -12

Power supplies. -5 is often not implimented.

AEN

Address Enable. This is asserted when a DMAC has control of the bus. This prevents an I/O device from responding to the I/O command lines during a DMA transfer.

BALE

Bus Address Latch Enable. The address bus is latched on the rising edge of this signal. The address on the SA bus is valid from the falling edge of BALE to the end of the bus cycle. Memory devices should latch the LA bus on the falling edge of BALE.

BCLK

Bus Clock, 33% Duty Cycle. Frequency Varies. 8.33 MHz is specified as the maximum, but many systems allow this clock to be set to 10 MHz and higher.

BE(x)

Byte Enable. Indicates to the slave device which bytes on the data bus contain valid data. A 16 bit transfer would assert BE0 and BE1, for example, but not BE2 or BE3.

CHCHK

Channel Check. A low signal generates an NMI. The NMI signal can be masked on a

PC, externally to the processor (of course). Bit 7 of port 70(hex) (enable NMI interrupts) and bit 3 of port 61 (hex) (recognition of channel check) must both be set to zero for an NMI to reach the cpu.

CHRDY

Channel Ready. Setting this low prevents the default ready timer from timing out. The slave device may then set it high again when it is ready to end the bus cycle. Holding this line low for too long can cause problems on some systems. CHRDY and NOWS should not be used simultaneously. This may cause problems with some bus controllers.

CMD

Command Phase. This signal indicates that the current bus cycle is in the command phase. After the start phase (see START), the data is transferred during the CMD phase. CMD remains asserted from the falling edge of START until the end of the bus cycle.

SD0-SD16

System Data lines. They are bidirectional and tri-state.

DAKx

DMA Acknowledge.

DRQx

DMA Request.

EX16

EISA Slave Size 16. This is used by the slave device to inform the bus master that it is capable of 16 bit transfers.

EX32

EISA Slave Size 32. This is used by the slave device to inform the bus master that it is capable of 32 bit transfers.

EXRDY

EISA Ready. If this signal is asserted, the cycle will end on the next rising edge of BCLK. The slave device drives this signal low to insert wait states.

IO16

I/O size 16. Generated by a 16 bit slave when addressed by a bus master.

IORC

I/O Read Command line.

IOWC

I/O Write Command line.

IRQx

Interrupt Request. IRQ2 has the highest priority.

LAxx

Latchable Address lines.

LOCK

Asserting this signal prevents other bus masters from requesting control of the bus.

MAKx

Master Acknowledge for slot x: Indicates that the bus master request (MREQx) has been granted.

MASTER16

16 bit bus master. Generated by the ISA bus master when initiating a bus cycle.

M/IO

Memory/Input-Output. This is used to indicate whether the current bus cycle is a memory or an I/O operation.

M16

Memory Access, 16 bit

MRDC

Memory Read Command line.

MREQx

Master Request for Slot x: This is a slot specific request for the device to become the bus master.

MSBURST

Master Burst. The bus master asserts this signal in response to SLBURST. This tells the slave device that the bus master is also capable of burst cycles.

MWTC

Memory Write Command line.

NOWS

No Wait State. Used to shorten the number of wait states generated by the default ready timer. This causes the bus cycle to end more quickly, since wait states will not be inserted. Most systems will ignore NOWS if CHRDY is active (low). However, this may cause problems with some bus controllers, and both signals should not be active simultaneously.

OSC

Oscillator, 14.318 MHz, 50% Duty Cycle. Frequency varies.

REFRESH

Refresh. Generated when the refresh logic is bus master.

RESDRV

This signal goes low when the machine is powered up. Driving it low will force a system reset.

SA0-SA19

System Address Lines, tri-state.

SBHE

System Bus High Enable, tristate. Indicates a 16 bit data transfer.

SLBURST

Slave Burst. The slave device uses this to indicate that it is capable of burst cycles. The bus master will respond with MSBURST if it is also capable of burst cycles.

SMRDC

Standard Memory Read Command line. Indicates a memory read in the lower 1 MB area.

SMWTC

Standard Memory Write Commmand line. Indicates a memory write in the lower 1 MB area.

START

Start Phase. This signal is low when the current bus cycle is in the start phase. Address and M/IO signals are decoded during this phase. Data is transferred during the command phase (indicated by CMD).

TC

Terminal Count. Notifies the cpu that that the last DMA data transfer operation is complete.

W/R

Write or Read. Used to indicate if the current bus cycle is a read or a write operation.

Contributor: Joakim Ogren, Mark Sokos

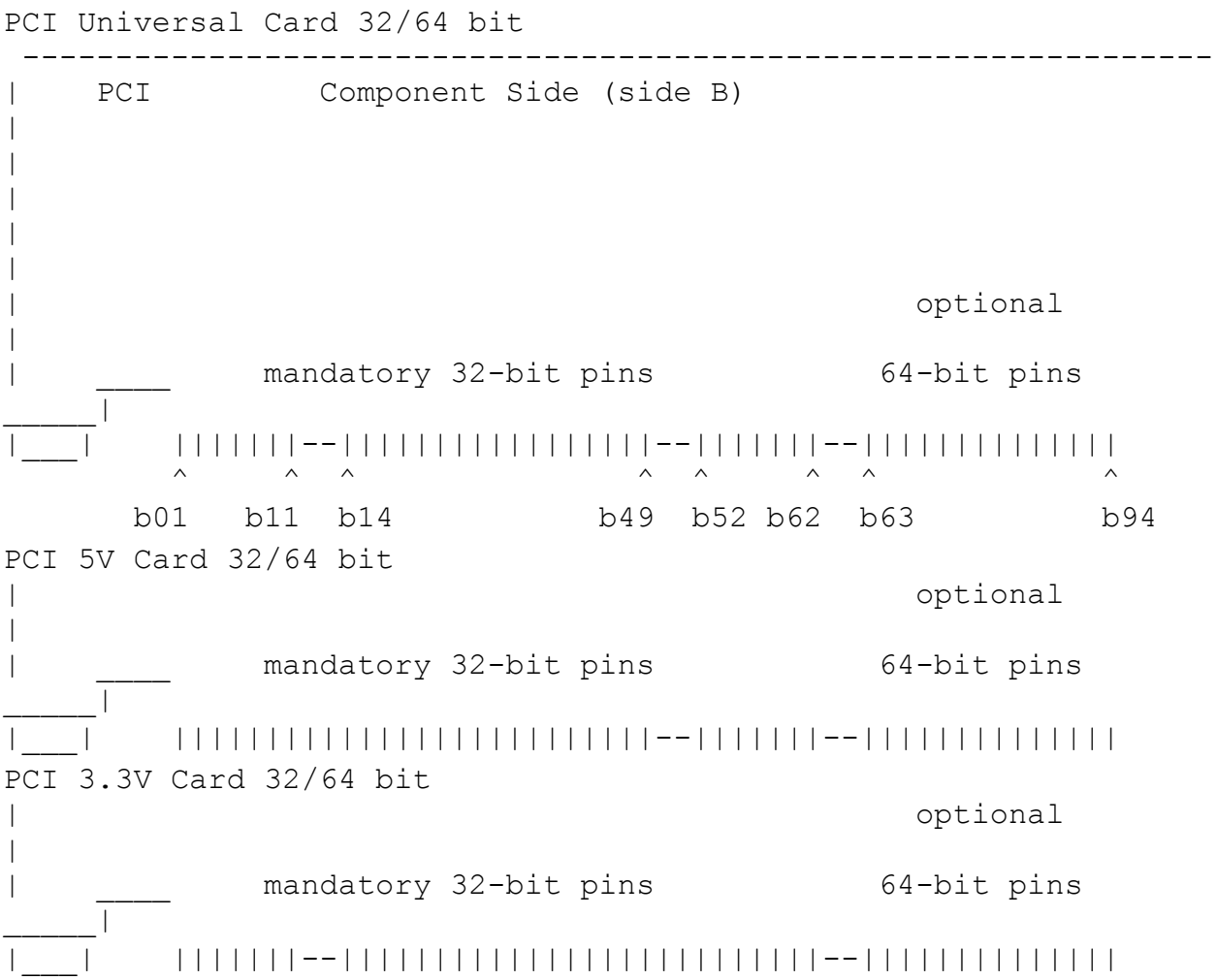
Sources:Mark Sokos EISA page
Sources:"Eisa System Architecture, 2nd Edition" by Tom Shanley and Don Anderson, ISBN 0-201-40995-X

Please send any comments to Joakim Ogren.

PCI Connector

PCI

PCI=Peripheral Component Interconnect



(At the computer)

98+22 PIN EDGE CONNECTOR at the computer.

Pin	+5V	+3.3V	Universal	Description
A1	TRST			Test Logic Reset
A2	+12V			+12 VDC
A3	TMS			Test Mde Select
A4	TDI			Test Data Input
A5	+5V			+5 VDC
A6	INTA			Interrupt A
A7	INTC			Interrupt C
A8	+5V			+5 VDC
A9	RESV01			Reserved VDC
A10	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A11	RESV03			Reserved VDC

A12	GND03	(OPEN)	(OPEN)	Ground or Open (Key)
A13	GND05	(OPEN)	(OPEN)	Ground or Open (Key)
A14	RESV05			Reserved VDC
A15	RESET			Reset
A16	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A17	GNT			Grant PCI use
A18	GND08			Ground
A19	RESV06			Reserved VDC
A20	AD30			Address/Data 30
A21	+3.3V01			+3.3 VDC
A22	AD28			Address/Data 28
A23	AD26			Address/Data 26
A24	GND10			Ground
A25	AD24			Address/Data 24
A26	IDSEL			Initialization Device Select
A27	+3.3V03			+3.3 VDC
A28	AD22			Address/Data 22
A29	AD20			Address/Data 20
A30	GND12			Ground
A31	AD18			Address/Data 18
A32	AD16			Address/Data 16
A33	+3.3V05			+3.3 VDC
A34	FRAME			Address or Data phase
A35	GND14			Ground
A36	TRDY			Target Ready
A37	GND15			Ground
A38	STOP			Stop Transfer Cycle
A39	+3.3V07			+3.3 VDC
A40	SDONE			Snoop Done
A41	SBO			Snoop Backoff
A42	GND17			Ground
A43	PAR			Parity
A44	AD15			Address/Data 15
A45	+3.3V10			+3.3 VDC
A46	AD13			Address/Data 13
A47	AD11			Address/Data 11
A48	GND19			Ground
A49	AD9			Address/Data 9
A52	C/BE0			Command, Byte Enable 0
A53	+3.3V11			+3.3 VDC
A54	AD6			Address/Data 6
A55	AD4			Address/Data 4
A56	GND21			Ground
A57	AD2			Address/Data 2
A58	AD0			Address/Data 0
A59	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A60	REQ64			Request 64 bit ???
A61	VCC11			+5 VDC
A62	VCC13			+5 VDC
A63	GND			Ground
A64	C/BE[7]#			Command, Byte Enable 7
A65	C/BE[5]#			Command, Byte Enable 5
A66	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A67	PAR64			Parity 64 ???
A68	AD62			Address/Data 62

A69	GND			Ground
A70	AD60			Address/Data 60
A71	AD58			Address/Data 58
A72	GND			Ground
A73	AD56			Address/Data 56
A74	AD54			Address/Data 54
A75	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A76	AD52			Address/Data 52
A77	AD50			Address/Data 50
A78	GND			Ground
A79	AD48			Address/Data 48
A80	AD46			Address/Data 46
A81	GND			Ground
A82	AD44			Address/Data 44
A83	AD42			Address/Data 42
A84	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A85	AD40			Address/Data 40
A86	AD38			Address/Data 38
A87	GND			Ground
A88	AD36			Address/Data 36
A89	AD34			Address/Data 34
A90	GND			Ground
A91	AD32			Address/Data 32
A92	RES			Reserved
A93	GND			Ground
A94	RES			Reserved
B1	-12V			-12 VDC
B2	TCK			Test Clock
B3	GND			Ground
B4	TDO			Test Data Output
B5	+5V			+5 VDC
B6	+5V			+5 VDC
B7	INTB			Interrupt B
B8	INTD			Interrupt D
B9	PRSNT1			Reserved
B10	RES			+V I/O (+5 V or +3.3 V)
B11	PRSNT1			??
B12	GND	(OPEN)	(OPEN)	Ground or Open (Key)
B13	GND	(OPEN)	(OPEN)	Ground or Open (Key)
B14	RES			Reserved VDC
B15	GND			Reset
B16	CLK			Clock
B17	GND			Ground
B18	REQ			Request
B19	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B20	AD31			Address/Data 31
B21	AD29			Address/Data 29
B22	GND			Ground
B23	AD27			Address/Data 27
B24	AD25			Address/Data 25
B25	+3.3V			+3.3VDC
B26	C/BE3			Command, Byte Enable 3
B27	AD23			Address/Data 23
B28	GND			Ground
B29	AD21			Address/Data 21

B30	AD19			Address/Data 19
B31	+3.3V			+3.3 VDC
B32	AD17			Address/Data 17
B33	C/BE2			Command, Byte Enable 2
B34	GND13			Ground
B35	IRDY			Initiator Ready
B36	+3.3V06			+3.3 VDC
B37	DEVSEL			Device Select
B38	GND16			Ground
B39	LOCK			Lock bus
B40	PERR			Parity Error
B41	+3.3V08			+3.3 VDC
B42	SERR			System Error
B43	+3.3V09			+3.3 VDC
B44	C/BE1			Command, Byte Enable 1
B45	AD14			Address/Data 14
B46	GND18			Ground
B47	AD12			Address/Data 12
B48	AD10			Address/Data 10
B49	GND20			Ground
B50	(OPEN)	GND	(OPEN)	Ground or Open (Key)
B51	(OPEN)	GND	(OPEN)	Ground or Open (Key)
B52	AD8			Address/Data 8
B53	AD7			Address/Data 7
B54	+3.3V12			+3.3 VDC
B55	AD5			Address/Data 5
B56	AD3			Address/Data 3
B57	GND22			Ground
B58	AD1			Address/Data 1
B59	VCC08			+5 VDC
B60	ACK64			Acknowledge 64 bit ???
B61	VCC10			+5 VDC
B62	VCC12			+5 VDC
B63	RES			Reserved
B64	GND			Ground
B65	C/BE[6]#			Command, Byte Enable 6
B66	C/BE[4]#			Command, Byte Enable 4
B67	GND			Ground
B68	AD63			Address/Data 63
B69	AD61			Address/Data 61
B70	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B71	AD59			Address/Data 59
B72	AD57			Address/Data 57
B73	GND			Ground
B74	AD55			Address/Data 55
B75	AD53			Address/Data 53
B76	GND			Ground
B77	AD51			Address/Data 51
B78	AD49			Address/Data 49
B79	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B80	AD47			Address/Data 47
B81	AD45			Address/Data 45
B82	GND			Ground
B83	AD43			Address/Data 43
B84	AD41			Address/Data 41

B85	GND			Ground
B86	AD39			Address/Data 39
B87	AD37			Address/Data 37
B88	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B89	AD35			Address/Data 35
B90	AD33			Address/Data 33
B91	GND			Ground
B92	RES			Reserved
B93	RES			Reserved
B94	GND			Ground

Notes: Pin 63-94 exists only on 64 bit PCI implementations.

+V I/O is 3.3V on 3.3V boards, 5V on 5V boards, and define signal rails on the Universal board.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

PCI (Technical)

This section is currently based soly on the work by Mark Sokos.

This file is not intended to be a thorough coverage of the PCI standard. It is for informational purposes only, and is intended to give designers and hobbyists an overview of the bus so that they might be able to design their own PCI cards. Thus, I/O operations are explained in the most detail, while memory operations, which will usually not be dealt with by an I/O card, are only briefly explained. Hobbyists are also warned that, due to the higher clock speeds involved, PCI cards are more difficult to design than ISA cards or cards for other slower busses. Many companies are now making PCI prototyping cards, and, for those fortunate enough to have access to FPGA programmers, companies like Xilinx are offering PCI compliant designs which you can use as a starting point for your own projects.

For a copy of the full PCI standard, contact:

PCI Special Interest Group (SIG)
PO Box 14070
Portland, OR 97214
1-800-433-5177
1-503-797-4207

Signal Descriptions:

AD(x)

Address/Data Lines.

CLK

Clock. 33 MHz maximum.

C/BE(x)

Command, Byte Enable.

FRAME

Used to indicate whether the cycle is an address phase or or a data phase.

DEVSEL

Device Select.

IDSEL

Initialization Device Select

INT(x)

Interrupt

IRDY

Initiator Ready

LOCK

Used to manage resource locks on the PCI bus.

REQ

Request. Requests a PCI transfer.

GNT

Grant. indicates that permission to use PCI is granted.

PAR

Parity. Used for AD0-31 and C/BE0-3.

PERR

Parity Error.

RST

Reset.

SBO

Snoop Backoff.

SDONE

Snoop Done.

SERR

System Error. Indicates an address parity error for special cycles or a system error.

STOP

Asserted by Target. Requests the master to stop the current transfer cycle.

TCK

Test Clock

TDI

Test Data Input

TDO

Test Data Output

TMS

Test Mode Select

TRDY

Target Ready

TRST

Test Logic Reset

The PCI bus treats all transfers as a burst operation. Each cycle begins with an address phase followed by one or more data phases. Data phases may repeat indefinately, but are limited by a timer that defines the maximum amount of time that the PCI device may control the bus. This timer is set by the CPU as part of the configuration space. Each device has its own timer (see the Latency Timer in the configuration space).

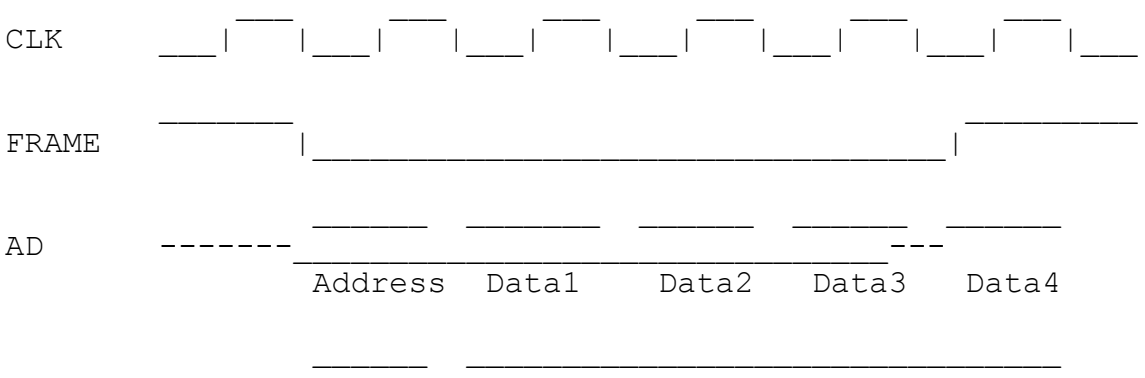
The same lines are used for address and data. The command lines are also used for byte enable lines. This is done to reduce the overall number of pins on the PCI connector.

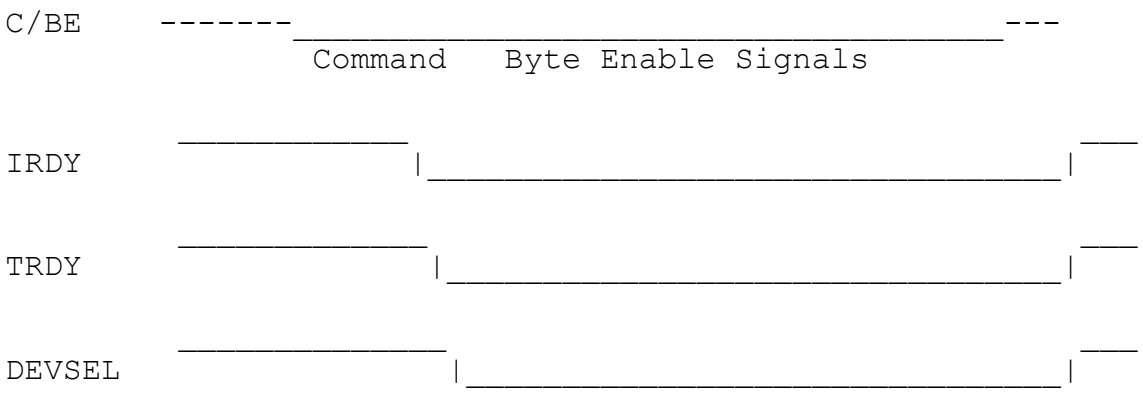
The Command lines (C/BE3 to C/BE0) indicate the type of bus transfer during the address phase.

C/BE	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	reserved
0101	reserved
0110	Memory Read
0111	Memory Write
1000	reserved
1001	reserved
1010	Configuration Read
1011	Configuration Write
1100	Multiple Memory Read
1101	Dual Address Cycle
1110	Memory-Read Line
1111	Memory Write and Invalidate

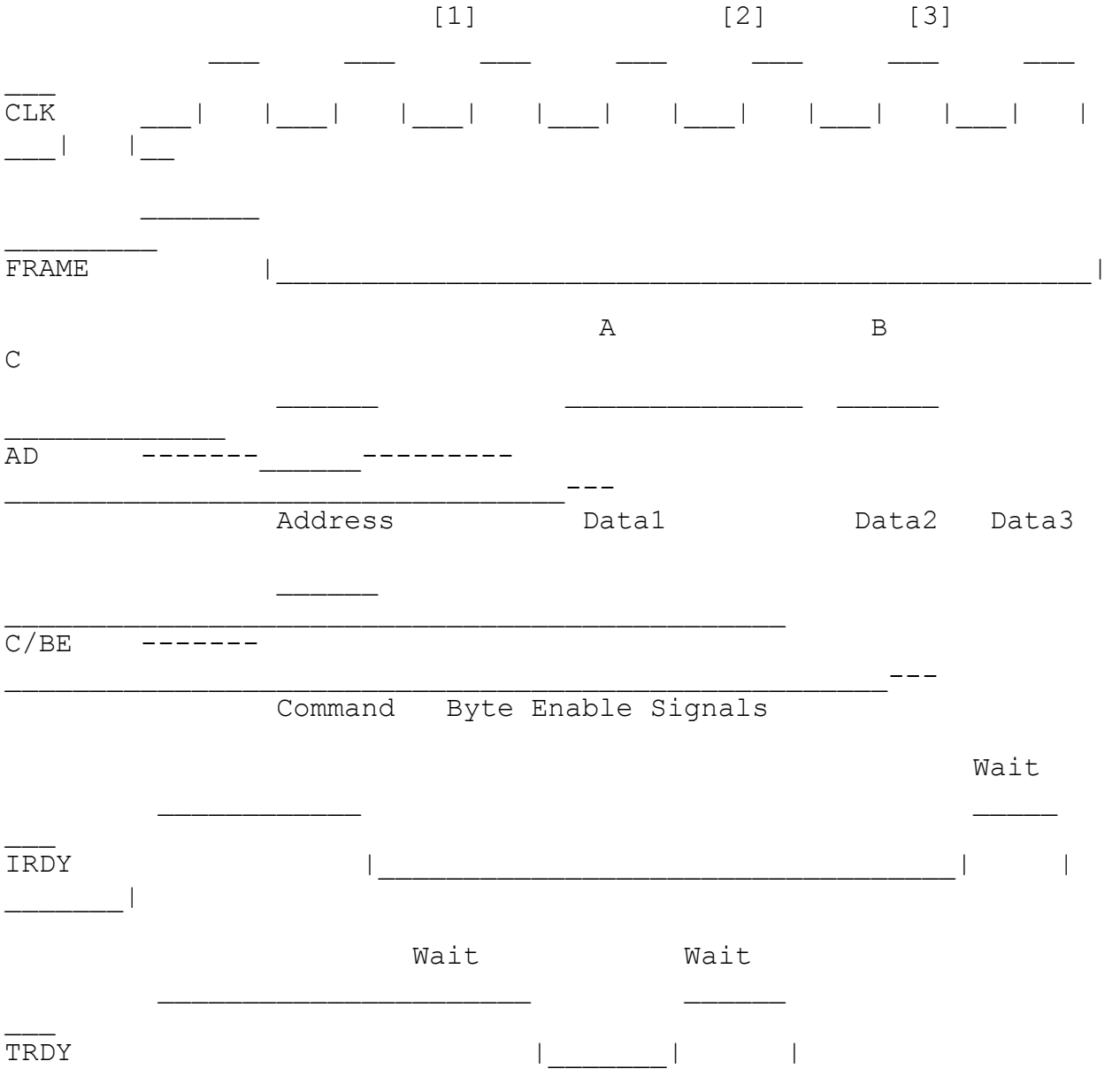
The three basic types of transfers are I/O, Memory, and Configuration.

PCI timing diagrams:





PCI transfer cycle, 4 data phases, no wait states. Data is transferred on the rising edge of CLK.



PCI transfer cycle, with wait states. Data is transferred on the rising edge of CLK at points labled A, B, and C.

Bus Cycles:

Interrupt Acknowledge (0000)

The interrupt controller automatically recognizes and reacts to the INTA (interrupt acknowledge) command. In the data phase, it transfers the interrupt vector to the AD lines.

Special Cycle (0001)

AD15-AD0	Description
0x0000	Processor Shutdown
0x0001	Processor Halt
0x0002	x86 Specific Code
0x0003 to 0xFFFF	Reserved

I/O Read (0010) and I/O Write (0011)

Input/Output device read or write operation. The AD lines contain a byte address (AD0 and AD1 must be decoded). PCI I/O ports may be 8 or 16 bits. PCI allows 32 bits of address space. On IBM compatible machines, the Intel CPU is limited to 16 bits of I/O space, which is further limited by some ISA cards that may also be installed in the machine (many ISA cards only decode the lower 10 bits of address space, and thus mirror themselves throughout the 16 bit I/O space). This limit assumes that the machine supports ISA or EISA slots in addition to PCI slots.

The PCI configuration space may also be accessed through I/O ports 0x0CF8 (Address) and 0x0CFC (Data). The address port must be written first.

Memory Read (0110) and Memory Write (0111)

A read or write to the system memory space. The AD lines contain a doubleword address. AD0 and AD1 do not need to be decoded. The Byte Enable lines (C/BE) indicate which bytes are valid.

Configuration Read (1010) and Configuration Write (1011)

A read or write to the PCI device configuration space, which is 256 bytes in length. It is accessed in doubleword units. AD0 and AD1 contain 0, AD2-7 contain the doubleword address, AD8-10 are used for selecting the addressed unit a the malfunction unit, and the remaining AD lines are not used.

```
Address     Bit 32      16   15           0

00          Unit ID        | Manufacturer ID
04          Status         | Command
08          Class Code               | Revision
0C          BIST  | Header | Latency | CLS
10-24            Base Address Register
28          Reserved
2C          Reserved
30          Expansion ROM Base Address
34          Reserved
38          Reserved
3C          MaxLat|MnGNT   | INT-pin | INT-line
40-FF       available for PCI unit
```

Multiple Memory Read (1100)

This is an extension of the memory read bus cycle. It is used to read large blocks of memory without caching, which is beneficial for long sequential memory accesses.

Dual Address Cycle (1101)

Two address cycles are necessary when a 64 bit address is used, but only a 32 bit physical address exists. The least significant portion of the address is placed on the AD lines first, followed by the most significant 32 bits. The second address cycle also contains the command for the type of transfer (I/O, Memory, etc). The PCI bus supports a 64 bit I/O address space, although this is not available on Intel based PCs due to limitations of the CPU.

Memory-Read Line (1110)

This cycle is used to read in more than two 32 bit data blocks, typically up to the end of a cache line. It is more effecient than normal memory read bursts for a long series of sequential memory accesses.

Memory Write and Invalidate (1111)

This indicates that a minimum of one cache line is to be transferred. This allows main memory to be updated, saving a cache write-back cycle.

Bus Arbitration:

This section is under construction.

PCI Bios:

This section is under construction.

Contributor: Joakim Ogren, Mark Sokos

Sources:Mark Sokos PCI page
Sources: "Inside the PCI Local Bus" by Guy W. Kendall, Byte, February 1994 v 19 p. 177-180

Sources: "The Indispensible PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3

Please send any comments to Joakim Ogren.

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http://www.gl.umbc.edu/~msokos1/pci.txt
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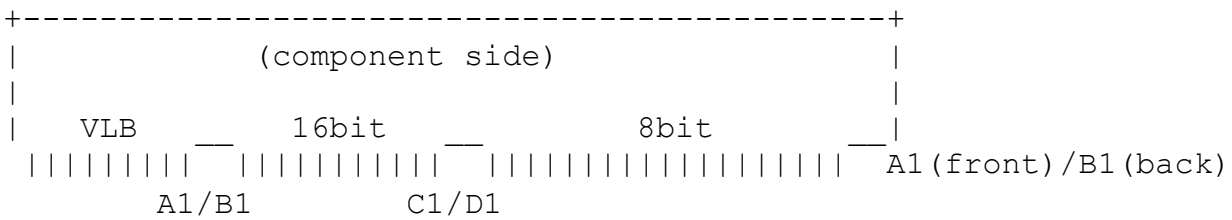
VESA LocalBus (VLB) Connector

NEW
NEW
NEW

VESA LocalBus (VLB)

VLB=VESA Local Bus.
VESA=Video Electronics Standards Association.



A=Component Side
B=Sold Side

NEW (At the computer)
58 PIN EDGE CONNECTOR at the computer.

Pin	Name	Description
A1	D1	Data 1
A2	D3	Data 3
A3	GND	Ground
A4	D5	Data 5
A5	D7	Data 7
A6	D9	Data 9
A7	D11	Data 11
A8	D13	Data 13
A9	D15	Data 15
A10	GND	Ground
A11	D17	Data 17
A12	Vcc	+5 VDC
A13	D19	Data 19
A14	D21	Data 21
A15	D23	Data 23
A16	D25	Data 25
A17	GND	Ground
A18	D27	Data 27
A19	D29	Data 2
A20	D31	Data 31
A21	A30	Address 30
A22	A28	Address 28
A23	A26	Address 26
A24	GND	Ground
A25	A24	Address 24
A26	A22	Address 22
A27	VCC	+5 VDC
A28	A20	Address 20
A29	A18	Address 18
A30	A16	Address 16
A31	A14	Address 14
A32	A12	Address 12

A33	A10	Address 10
A34	A8	Address 8
A35	GND	Ground
A36	A6	Address 6
A37	A4	Address 4
A38	WBACK#	Write Back
A39	BE0#	Byte Enable 0
A40	VCC	+5 VDC
A41	BE1#	Byte Enable 1
A42	BE2#	Byte Enable 2
A43	GND	Ground
A44	BE3#	Byte Enable 3
A45	ADS#	Address Strobe
A48	LRDY#	Local Ready
A49	LDEV	Local Device
A50	LREQ	Local Request
A51	GND	Ground
A52	LGNT	Local Grant
A53	VCC	+5 VDC
A54	ID2	Identification 2
A55	ID3	Identification 3
A56	ID4	Identification 4
A57	LKEN#	
A58	LEADS#	Local Enable Address Strobe
B1	D0	Data 0
B2	D2	Data 2
B3	D4	Data 4
B4	D6	Data 6
B5	D8	Data 8
B6	GND	Ground
B7	D10	Data 10
B8	D12	Data 12
B9	VCC	+5 VDC
B10	D14	Data 14
B11	D16	Data 16
B12	D18	Data 18
B13	D20	Data 20
B14	GND	Ground
B15	D22	Data 22
B16	D24	Data 24
B17	D26	Data 26
B18	D28	Data 28
B19	D30	Data 30
B20	VCC	+5 VDC
B21	A31	Address 31
B22	GND	Ground
B23	A29	Address 29
B24	A27	Address 27
B25	A25	Address 25
B26	A23	Address 23
B27	A21	Address 21
B28	A19	Address 19
B29	GND	Ground
B30	A17	Address 17

B31	A15	Address 15
B32	VCC	+5 VDC
B33	A13	Address 13
B34	A11	Address 11
B35	A9	Address 9
B36	A7	Address 7
B37	A5	Address 5
B38	GND	Ground
B39	A3	Address 3
B40	A2	Address 2
B41	n/c	Not connected
B42	RESET#	Reset
B43	DC#	Data/Command
B44	M/IO#	Memory/IO
B45	W/R#	Write/Read
B48	RDYRTN#	Ready Return
B49	GND	Ground
B50	IRQ9	Interrupt 9
B51	BRDY#	Burst Ready
B52	BLAST#	Burst Last
B53	ID0	Identification 0
B54	ID1	Identification 1
B55	GND	Ground
B56	LCLK	Local Clock
B57	VCC	+5 VDC
B58	LBS16#	Local Bus Size 16

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

VESA LocalBus (VLB) (Technical)

This section is currently based soly on the work by Mark Sokos.

This file is intended to provide a basic functional overview of the Vesa Local Bus, so that hobbyists and ametuers can design their own VLB compatible cards.

It is not intended to provide complete coverage of the VLB standard.

VLB Connectors are usually inline with ISA connectors, so that adapter cards may use both. However, the VLB is seperate, and does not need to connect to the ISA portion of the bus.

The 64 bit expansion of the bus (optional) does not add additional pins or connectors. Instead, it multiplexes the existing pins. The 32 bit VLB bus does not use the 64 bit signals shown in the above pinouts.

Signal Descriptions

A2-A31

Address Bus

ADS

Address Strobe

BE0-BE3

Byte Enable. Indicates that the 8 data lines corresponding to each signal will deliver valid data.

BLAST

Burst Last. Indicates a VLB Burst Cycle, which will complete with *BRDY. The VLB Burst cycle consists of an address phase followed by four data phases.

BRDY

Burst Ready. Indicates the end of the current burst transfer.

D0-D31

Data Bus. Valid bytes are indicated by *BE(x) signals.

D/C

Data/Command. Used with M/IO and W/R to indicate the type of cycle.

M/IO	D/C	W/R	
0	0	0	INTA sequence
0	0	1	Halt/Special (486)
0	1	0	I/O Read

0	1	1	I/O Write
1	0	0	Instruction Fetch
1	0	1	Halt/Shutdown (386)
1	1	0	Memory Read
1	1	1	Memory Write

ID0-ID4

Identification Signals.

ID0	ID1	ID4	CPU
0	0	0	(res)
0	0	1	(res)
0	1	0	486
0	1	1	486
1	0	0	386
1	0	1	386
1	1	0	(res)
1	1	1	486

ID2 Indicates wait:	0 = 1 wait cycle (min) 1 = no wait
ID3 Indicates bus speed:	0 = greater than 33.3 MHz 1 = less than 33.3 MHz

IRQ9

Interrupt Request. Connected to IRQ9 on ISA bus.This allows standalone VLB adapters (not connected to ISA portion of the bus) to have one IRQ.

LEADS

Local Enable Address Strobe. Set low by VLB master (not CPU). Also used for cache invalidation signal.

LBS16

Local Bus Size 16. Used by slave device to indicate that it has a transfer width of only 16 bits.

LCLK

Local Clock. Runs at the same frequency as the cpu, up to 50 MHz. 66 MHz is allowed for on-board devices.

LDEV

Local Device: When appropriate address and M/IO signals are present on the bus, the VLB device must pull this line low to indicate that it is a VLB device. The VLB controller will then use the VLB bus for the transfer.

LRDY

Local Ready. Indicates that the VLB device has completed the cycle. This signal is only used for single cycle transfers. *BRDY is used for burst transfers.

LGNT

Local Grant. Indicates that an *LREQ signal has been granted, and control is being transferred to the new VLB master.

LREQ

Local Request. Used by VLB Master to gain control of the bus.

M/IO

Memory/IO. See D/C for signal description.

RDYRTN

Ready Return. Indicates VLB cycle has been completed. May precede LRDY by one cycle.

RESET

Reset. Resets all VLB devices.

WBACK

Write Back.

64-bit Expansion Signals

ACK64

Acknowledge 64 bit transfer. Indicates that the device can perform the requested 64 bit transfer cycle.

BE4-BE7

Byte Enable. Indicates which bytes are valid (similar to BE0-BE3).

D32-D63

Upper 32 bits of data bus. Multiplexed with address bus.

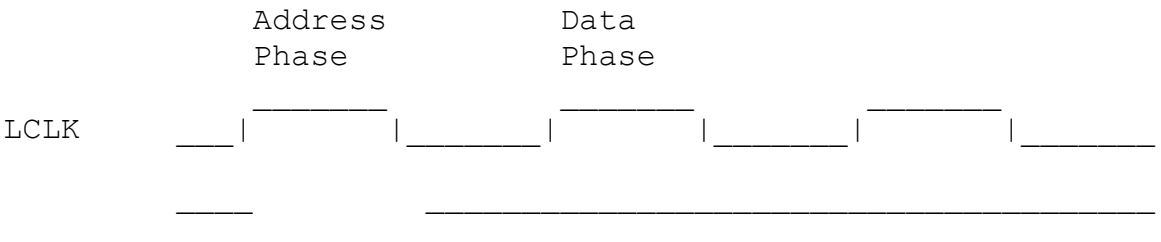
LBS64

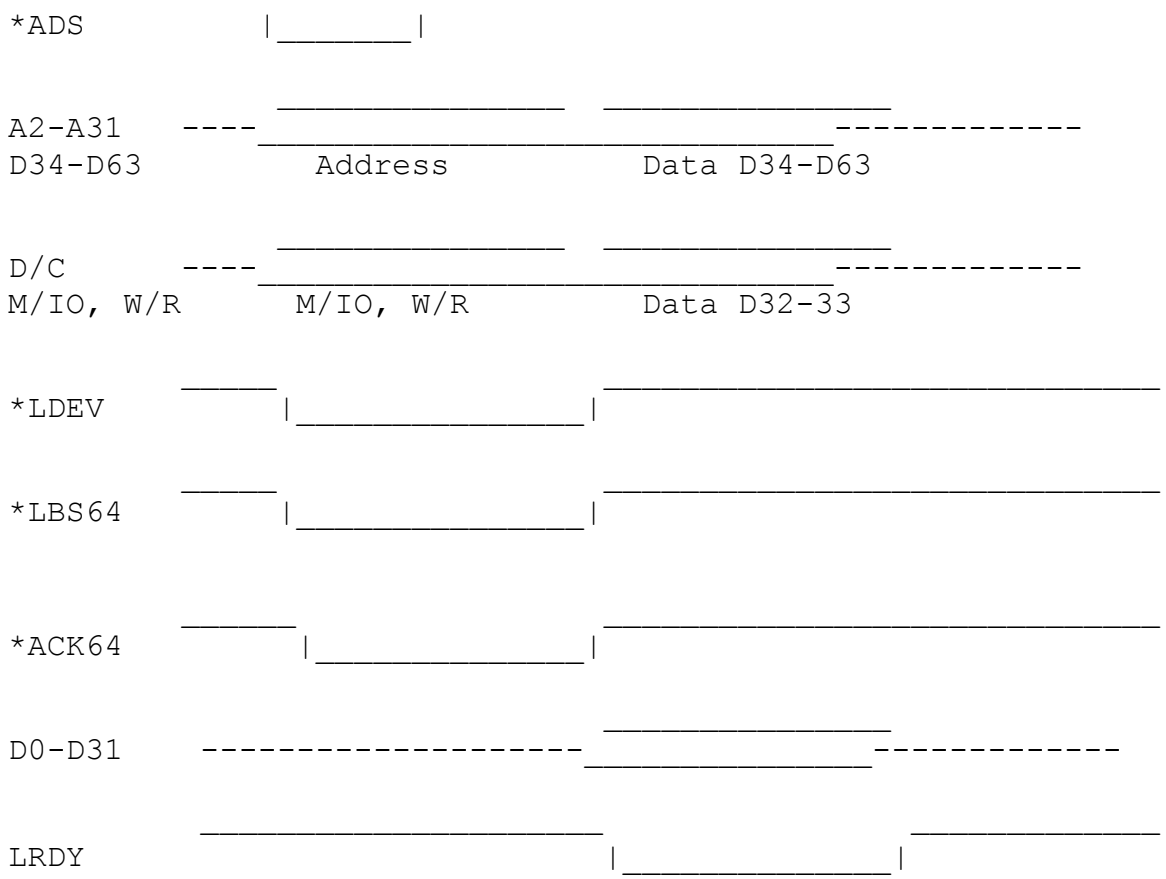
Local Bus Size 64 bits. Used by VLB Master to indicate that it desires a 64 bit transfer.

W/R

Write/Read. See D/C for signal description.

64 Bit Data Transfer Timing Diagram:





Contributor: Joakim Ogren, Mark Sokos

Sources:Mark Sokos VLB page
Sources:"The Indispensible PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3

Please send any comments to Joakim Ogren.

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CompactPCI Connector

NEW
NEW
NEW

CompactPCI

PCI=Peripheral Component Interconnect.
CompactPCI is a a version of PCI adapted for industrial and/or embedded applications.

NEW (At the backplane)

NEW (At the device (card))

7x47 PIN (IEC917 and IEC1076-4-101) CONNECTOR at the backplane.
7x47 PIN (IEC917 and IEC1076-4-101) CONNECTOR at the device (card).

Pin	Name	Description
Z1	GND	Ground
Z2	GND	Ground
Z3	GND	Ground
Z4	GND	Ground
Z5	GND	Ground
Z6	GND	Ground
Z7	GND	Ground
Z8	GND	Ground
Z9	GND	Ground
Z10	GND	Ground
Z11	GND	Ground
Z12	KEY	Keyed (no pin)
Z13	KEY	Keyed (no pin)
Z14	KEY	Keyed (no pin)
Z15	GND	Ground
Z16	GND	Ground
Z17	GND	Ground
Z18	GND	Ground
Z19	GND	Ground
Z20	GND	Ground
Z21	GND	Ground
Z22	GND	Ground
Z23	GND	Ground
Z24	GND	Ground
Z25	GND	Ground
Z26	GND	Ground
Z27	GND	Ground
Z28	GND	Ground
Z29	GND	Ground
Z30	GND	Ground
Z31	GND	Ground
Z32	GND	Ground
Z33	GND	Ground
Z34	GND	Ground
Z35	GND	Ground
Z36	GND	Ground
Z37	GND	Ground
Z38	GND	Ground
Z39	GND	Ground

Z40	GND	Ground
Z41	GND	Ground
Z42	GND	Ground
Z43	GND	Ground
Z44	GND	Ground
Z45	GND	Ground
Z46	GND	Ground
Z47	GND	Ground

A1	5V	+5 VDC
A2	TCK	Test Clock
A3	INTA#	Interrupt A
A4	BRSV	Bused Reserved (don't use)
A5	BRSV	Bused Reserved (don't use)
A6	REQ#	Request PCI transfer
A7	AD(30)	Address/Data 30
A8	AD(26)	Address/Data 26
A9	C/BE(3)#	Command: Byte Enable
A10	AD(21)	Address/Data 21
A11	AD(18)	Address/Data 18
A12	KEY	Keyed (no pin)
A13	KEY	Keyed (no pin)
A14	KEY	Keyed (no pin)
A15	3.3V	+3.3 VDC
A16	DEVSEL#	Device Select
A17	3.3V	+3.3 VDC
A18	SERR#	System Error
A19	3.3V	+3.3 VDC
A20	AD(12)	Address/Data 12
A21	3.3V	+3.3 VDC
A22	AD(7)	Address/Data 7)
A23	3.3V	+3.3 VDC
A24	AD(1)	Address/Data 1)
A25	5V	+5 VDC
A26	CLK1	Clock ?? MHz
A27	CLK2	Clock ?? MHz
A28	CLK4	Clock ?? MHz
A29	V(I/O)	+3.3 VDC or +5 VDC
A30	C/BE(5)#	Command: Byte Enable
A31	AD(63)	Address/Data 63
A32	AD(59)	Address/Data 59
A33	AD(56)	Address/Data 56
A34	AD(52)	Address/Data 52
A35	AD(49)	Address/Data 49
A36	AD(45)	Address/Data 45
A37	AD(42)	Address/Data 42
A38	AD(38)	Address/Data 38
A39	AD(35)	Address/Data 35
A40	BRSV	Bused Reserved (don't use)
A41	BRSV	Bused Reserved (don't use)
A42	BRSV	Bused Reserved (don't use)
A43	USR	User Defined
A44	USR	User Defined
A45	USR	User Defined
A46	USR	User Defined
A47	USR	User Defined

B1	-12V	-12 VDC
B2	5V	+5 VDC
B3	INTB#	Interrupt B
B4	GND	Ground
B5	BRSV	Bused Reserved (don't use)
B6	GND	Ground
B7	AD(29)	Address/Data 29
B8	GND	Ground
B9	IDSEL	Initialization Device Select
B10	GND	Ground
B11	AD(17)	Address/Data 17
B12	KEY	Keyed (no pin)
B13	KEY	Keyed (no pin)
B14	KEY	Keyed (no pin)
B15	FRAME#	Address or Data phase
B16	GND	Ground
B17	SDONE	Snoop Done
B18	GND	Ground
B19	AD(15)	Address/Data 15
B20	GND	Ground
B21	AD(9)	Address/Data 9)
B22	GND	Ground
B23	AD(4)	Address/Data 4)
B24	5V	+5 VDC
B25	REQ64#	
B26	GND	Ground
B27	CLK3	Clock ?? MHz
B28	GND	Ground
B29	BRSV	Bused Reserved (don't use)
B30	GND	Ground
B31	AD(62)	Address/Data 62
B32	GND	Ground
B33	AD(55)	Address/Data 55
B34	GND	Ground
B35	AD(48)	Address/Data 48
B36	GND	Ground
B37	AD(41)	Address/Data 41
B38	GND	Ground
B39	AD(34)	Address/Data 34
B40	GND	Ground
B41	BRSV	Bused Reserved (don't use)
B42	GND	Ground
B43	USR	User Defined
B44	USR	User Defined
B45	USR	User Defined
B46	USR	User Defined
B47	USR	User Defined
C1	TRST#	Test Logic Reset
C2	TMS	Test Mode Select
C3	INTC#	Interrupt C
C4	V(I/O)	+3.3 VDC or +5 VDC
C5	RST	Reset
C6	3.3V	+3.3 VDC
C7	AD(28)	Address/Data 28

C8	V(I/O)	+3.3 VDC or +5 VDC
C9	AD(23)	Address/Data 23
C10	3.3V	+3.3 VDC
C11	AD(16)	Address/Data 16
C12	KEY	Keyed (no pin)
C13	KEY	Keyed (no pin)
C14	KEY	Keyed (no pin)
C15	IRDY#	Initiator Ready
C16	V(I/O)	+3.3 VDC or +5 VDC
C17	SBO#	Snoop Backoff
C18	3.3V	+3.3 VDC
C19	AD(14)	Address/Data 14
C20	V(I/O)	+3.3 VDC or +5 VDC
C21	AD(8)	Address/Data 8)
C22	3.3V	+3.3 VDC
C23	AD(3)	Address/Data 3)
C24	V(I/O)	+3.3 VDC or +5 VDC
C25	BRSV	Bused Reserved (don't use)
C26	REQ1#	Request PCI transfer
C27	SYSEN#	
C28	GNT3#	Grant
C29	C/BE(7)	Command: Byte Enable
C30	V(I/O)	+3.3 VDC or +5 VDC
C31	AD(61)	Address/Data 61
C32	V(I/O)	+3.3 VDC or +5 VDC
C33	AD(54)	Address/Data 54
C34	V(I/O)	+3.3 VDC or +5 VDC
C35	AD(47)	Address/Data 47
C36	V(I/O)	+3.3 VDC or +5 VDC
C37	AD(40)	Address/Data 40
C38	V(I/O)	+3.3 VDC or +5 VDC
C39	AD(33)	Address/Data 33
C40	FAL#	Power Supply Status FAL (CompactPCI specific)
C41	DEG#	Power Supply Status DEG (CompactPCI specific)
C42	PRST#	Push Button Reset (CompactPCI specific)
C43	USR	User Defined
C44	USR	User Defined
C45	USR	User Defined
C46	USR	User Defined
C47	USR	User Defined
D1	+12V	+12 VDC
D2	TDO	Test Data Output
D3	5V	+5 VDC
D4	INTP	
D5	GND	Ground
D6	CLK	
D7	GND	Ground
D8	AD(25)	Address/Data 25
D9	GND	Ground
D10	AD(20)	Address/Data 20
D11	GND	Ground
D12	KEY	Keyed (no pin)
D13	KEY	Keyed (no pin)
D14	KEY	Keyed (no pin)
D15	GND	Ground

D16	STOP#	Stop transfer cycle
D17	GND	Ground
D18	PAR	Parity for AD0-31 & C/BE0-3
D19	GND	Ground
D20	AD(11)	Address/Data 11
D21	M66EN	
D22	AD(6)	Address/Data 6)
D23	5V	+5 VDC
D24	AD(0)	Address/Data 0)
D25	3.3V	+3.3 VDC
D26	GNT1#	Grant
D27	GNT2#	Grant
D28	REQ4#	Request PCI transfer
D29	GND	Ground
D30	C/BE(4)#	Command: Byte Enable
D31	GND	Ground
D32	AD(58)	Address/Data 58
D33	GND	Ground
D34	AD(51)	Address/Data 51
D35	GND	Ground
D36	AD(44)	Address/Data 44
D37	GND	Ground
D38	AD(37)	Address/Data 37
D39	GND	Ground
D40	REQ5#	Request PCI transfer
D41	GND	Ground
D42	REQ6#	Request PCI transfer
D43	USR	User Defined
D44	USR	User Defined
D45	USR	User Defined
D46	USR	User Defined
D47	USR	User Defined

E1	5V	+5 VDC
E2	TDI	Test Data Input
E3	INTD#	Interrupt D
E4	INTS	
E5	GNT#	Grant
E6	AD(31)	Address/Data 31
E7	AD(27)	Address/Data 27
E8	AD(24)	Address/Data 24
E9	AD(22)	Address/Data 22
E10	AD(19)	Address/Data 19
E11	C/BE(2)#	Command: Byte Enable
E12	KEY	Keyed (no pin)
E13	KEY	Keyed (no pin)
E14	KEY	Keyed (no pin)
E15	TRDY#	Target Ready
E16	LOCK#	Lock resource
E17	PERR#	Parity Error
E18	C/BE(1)#	Command: Byte Enable
E19	AD(13)	Address/Data 13
E20	AD(10)	Address/Data 10
E21	C/BE(0)#	Command: Byte Enable
E22	AD(5)	Address/Data 5)
E23	AD(2)	Address/Data 2)

E24	ACK64#	
E25	5V	+5 VDC
E26	REQ2#	Request PCI transfer
E27	REQ3#	Request PCI transfer
E28	GNT4#	Grant
E29	C/BE(6)#	Command: Byte Enable
E30	PAR64	
E31	AD(60)	Address/Data 60
E32	AD(57)	Address/Data 57
E33	AD(53)	Address/Data 53
E34	AD(50)	Address/Data 50
E35	AD(46)	Address/Data 46
E36	AD(43)	Address/Data 43
E37	AD(39)	Address/Data 39
E38	AD(36)	Address/Data 36
E39	AD(32)	Address/Data 32
E40	GNT5#	Grant
E41	BRSV	Bused Reserved (don't use)
E42	GNT6#	Grant
E43	USR	User Defined
E44	USR	User Defined
E45	USR	User Defined
E46	USR	User Defined
E47	USR	User Defined

F1	GND	Ground
F2	GND	Ground
F3	GND	Ground
F4	GND	Ground
F5	GND	Ground
F6	GND	Ground
F7	GND	Ground
F8	GND	Ground
F9	GND	Ground
F10	GND	Ground
F11	GND	Ground
F12	KEY	Keyed (no pin)
F13	KEY	Keyed (no pin)
F14	KEY	Keyed (no pin)
F15	GND	Ground
F16	GND	Ground
F17	GND	Ground
F18	GND	Ground
F19	GND	Ground
F20	GND	Ground
F21	GND	Ground
F22	GND	Ground
F23	GND	Ground
F24	GND	Ground
F25	GND	Ground
F26	GND	Ground
F27	GND	Ground
F28	GND	Ground
F29	GND	Ground
F30	GND	Ground
F31	GND	Ground

F32	GND	Ground
F33	GND	Ground
F34	GND	Ground
F35	GND	Ground
F36	GND	Ground
F37	GND	Ground
F38	GND	Ground
F39	GND	Ground
F40	GND	Ground
F41	GND	Ground
F42	GND	Ground
F43	GND	Ground
F44	GND	Ground
F45	GND	Ground
F46	GND	Ground
F47	GND	Ground

Contributor: Joakim Ogren

Sources:CompactPCI specifictions v1.0 at CompactPCI's homepage
Sources:Mark Sokos PCI page
Sources: "Inside the PCI Local Bus" by Guy W. Kendall, Byte, February 1994 v 19 p. 177-180
Sources: "The Indispensible PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.compactpci.com/cspec.htm
Open this address in your WWW browser.

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http://www.compactpci.com/
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CompactPCI (Technical)

This section does not currently contain so much in depth information as I would like.

Since CompactPCI is based on PCI you should first refer to the PCI standard. This only explains the extensions CompactPCI specifies.

For a copy of the full CompactPCI standard, contact:

PCI Industrial Computer Manufacturers Group (PICMG)
c/o Roger Communications
301 Edgewater place
Suite 220
Wakewater
MA01880
Phone: 1-617-224-1100
Fax: 1-617-224-1239

Overview:

A CompactPCI system is composed of up to eight CompactPCI card locations:

- One System Slot
- Up to seven Peipherial Slots

The connector has 7 columns with 47 rows. They're divided into groups:

- Row 1-25: 32-bit PCI
- Row 26-47: Additional pins for 64-bit PCI (System Slot boards must use it).
- Row 26-28 and 40-42: Primarily implemented on System Slot boards.

The following signals must be terminated:

- AD0-31
- C/BE0#-C/BE3#
- PAR
- FRAME#
- IRDY#
- TRDY#
- STOP#
- LOCK#
- IDSEL
- DEVSEL#
- PERR#
- SERR#
- RST#

The following signals must be terminated if used:

- INTA#
- INTB#
- INTC#

- INTD#
- SB0#
- SDOBE
- AD32-AD63
- C/BE4#-C/BE7#
- REQ64#
- ACK64#
- PAR64#

The following signals do no require a stub termination:

- CLK
- REQ#
- GNT#
- TDI#
- TDO
- TCK
- TMS
- TRST#

The System Slot board must pullup the following signals (even if not used):

- REQ64#
- ACK64#

Connector:

1	GND	5V	-12V	TRST#	12V	5V	GND
2	GND	TCK	5V	TMS	DO	TDI	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
4	GND	BRSV	GND	V(I/O)	INTP	INTS	GND
5	GND	BRSV	BRSV	RST	GND	GNT#	GND
6	GND	REQ#	GND	3.3V	CLK	AD(31)	GND
7	GND	AD(30)	AD(29)	AD(28)	GND	AD(27)	GND
8	GND	AD(26)	GND	V(I/O)	AD(25)	AD(24)	GND
9	GND	C/BE(3)#	IDSEL	AD(23)	GND	AD(22)	GND
10	GND	AD(21)	GND	3.3V	AD(20)	AD(19)	GND
11	GND	AD(18)	AS(17)	AD(16)	GND	C/BE(2)#	GND
12	KEY	KEY	KEY	KEY	KEY	KEY	KEY
13	KEY	KEY	KEY	KEY	KEY	KEY	KEY
14	KEY	KEY	KEY	KEY	KEY	KEY	KEY
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND

17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE(1)#	GND
19	GND	3.3V	AD(15)	AD(14)	GND	AD(13)	GND
20	GND	AD(12)	GND	V(I/O)	AD(11)	AD(10)	GND
21	GND	3.3V	AD(9)	AD(8)	M66EN	C/BE(0)#	GND
22	GND	AD(7)	GND	3.3V	AD(6)	AD(5)	GND
23	GND	3.3V	AD(4)	AD(3)	5V	AD(2)	GND
24	GND	AD(1)	5V	V(I/O)	AD(0)	ACK64#	GND
25	GND	5V	REQ64#	BRSV	3.3V	5V	GND
26	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
27	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
28	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
29	GND	V(I/O)	BRSV	C/BE(7)	GND	C/BE(6)#	GND
30	GND	C/BE(5)#	GND	V(I/O)	C/BE(4)#	PAR64	GND
31	GND	AD(63)	AD(62)	AD(61)	GND	AD(60)	GND
32	GND	AD(59)	GND	V(I/O)	AD(58)	AD(57)	GND
33	GND	AD(56)	AD(55)	AD(54)	GND	AD(53)	GND
34	GND	AD(52)	GND	V(I/O)	AD(51)	AD(50)	GND
35	GND	AD(49)	AD(48)	AD(47)	GND	AD(46)	GND
36	GND	AD(45)	GND	V(I/O)	AD(44)	AD(43)	GND
37	GND	AD(42)	AD(41)	AD(40)	GND	AD(39)	GND
38	GND	AD(38)	GND	V(I/O)	AD(37)	AD(36)	GND
39	GND	AD(35)	AD(34)	AD(33)	GND	AD(32)	GND
40	GND	BRSV	GND	FAL#	REQ5#	GNT5#	GND
41	GND	BRSV	BRSV	DEG#	GND	BRSV	GND
42	GND	BRSV	GND	PRST#	REQ6#	GNT6#	GND
43	GND	USR	USR	USR	USR	USR	GND
44	GND	USR	USR	USR	USR	USR	GND

45	GND	USR	USR	USR	USR	USR	GND
46	GND	USR	USR	USR	USR	USR	GND
47	GND	USR	USR	USR	USR	USR	GND
	Z	**A**	**B**	**C**	**D**	**E**	**F**

Signal Descriptions:

PRST

Push Button Reset.

DEG

Power Supply Status DEG

FAL

Power Supply Status FAL

SYSEN

System Slot Identification

Contributor: Joakim Ogren, Mark Sokos

Sources:CompactPCI specifictions v1.0 at CompactPCI's homepage
Sources:Mark Sokos PCI page
Sources: "Inside the PCI Local Bus" by Guy W. Kendall, Byte, February 1994 v 19 p. 177-180
Sources: "The Indispensible PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3

Info:CompactPCI - An Open Industrial Computer Standard article by Joseph S. Pavlat

Please send any comments to Joakim Ogren.

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IndustrialPCI Connector

NEW
NEW
NEW

IndustrialPCI (IPCI)

PCI=Peripheral Component Interconnect.
IndustrialPCI is a a version of PCI adapted for industrial and/or embedded applications.
The IPCI connector has three parts:

- Optional 60 pin PCI 64 bit extension (Top)
- Mandatory 120 pin PCI 32 bit (Middle)
- Optional 60 pin Custom I/O (Bottom)

NEW (At the backplane)

NEW (At the device (card))
UNKNOWN CONNECTOR at the backplane.
UNKNOWN CONNECTOR at the device (card).

System Slot (Middle)

Pin	Name	Description	Note
A1	+3,3V	+3.3 VDC	
A2	AD2	Address 2	
A3	AD6	Address 6	
A4	GND	Ground	
A5	AD10	Address 10	
A6	AD13	Address 13	
A7	GND	Ground	
A8	SDONE	Snoop Done	1
A9	GND	Ground	
A10	FRAME#	Indicate Address or Data phase	1
A11	AD18	Address 18	
A12	GND	Ground	
A13	+5V	+5 VDC	
A14	AD24	Address 24	
A15	AD27	Address 27	
A16	GND	Ground	
A17	REQ2	Request 2	1
A18	GND	Ground	
A19	CLK1	33 or 66 MHz Clock	
A20	CLK2		
A21	GND	Ground	
A22	CLK3		
A23	CLK4		
A24	+3,3V	+3.3 VDC	
B1	REQ64#	Request 64 ???	1
B2	AD3	Address 3	
B3	+5V	+5 VDC	
B4	AD8	Address 8	
B5	+3,3V	+3.3 VDC	
B6	AD14	Address 14	
B7	PAR	Parity	

B8	+3,3V	+3.3 VDC	
B9	STOP#	Stop	1
B10	C/BE2#	Command, Byte Enable 2	
B11	V(I/O)	+3.3 or +5 VDC	
B12	AD21	Address 21	
B13	+3,3V	+3.3 VDC	
B14	V(I/O)	+3.3 or +5 VDC	
B15	AD28	Address 28	
B16	AD31	Address 31	
B17	+3,3V	+3.3 VDC	
B18	GNT3	Grant 3	
B19	RST#	Reset	
B20	NMI#	Non Maskable Interrupt	
B21	X6	Reserved (6)	
B22	+5V	+5 VDC	:
B23	RSTIN#		2
B24	USB+	Universal Serial Bus (USB)(+)	
C1	ACK64#	Acknowledge 64 ???	1
C2	GND	Ground	
C3	AD7	Address 7	
C4	AD9	Address 9	
C5	AD11	Address 11	
C6	GND	Ground	
C7	SERR#	System Error	1
C8	PERR#	Parity Error	1
C9	DEVSEL#	Device Select	1
C10	GND	Ground	
C11	AD19	Address 19	
C12	AD22	Address 22	
C13	GND	Ground	
C14	AD25	Address 25	
C15	GND	Ground	
C16	X1	Reserved (1)	
C17	GNT2	Grant 2	
C18	REQ4	Request 4	1
C19	SLEEP#/SDAT	Sleep/Serial Data (I2C)	3
C20	X4	Reserved (4)	
C21	INTD#	Interrupt D	1
C22	INTB#	Interrupt B	1
C23	+5V	+5 VDC	
C24	USB-	Universal Serial Bus (USB)(-)	
D1	AD0	Address 0	
D2	AD4	Address 4	
D3	C/BE0#	Command, Byte Enable 0	
D4	+3,3V	+3.3 VDC	
D5	AD12	Address 12	
D6	AD15	Address 15	
D7	V(I/O)	+3.3 or +5 VDC	
D8	LOCK#	Resource Lock	1
D9	TRDY#	Test Logic Ready	1
D10	AD16	Address 16	
D11	AD20	Address 20	
D12	+5V	+5 VDC	
D13	+5V	+5 VDC	
D14	AD26	Address 26	
D15	AD29	Address 29	

D16	REQ1	Request 1	1
D17	REQ3	Request 3	1
D18	V(I/O)	+3.3 or +5 VDC	
D19	X2	Reserved (2)	
D20	X5	Reserved (5)	
D21	+3,3V	+3.3 VDC	
D22	INTA#	Interrupt A	1
D23	ICPEN#/SCLK	ICPEN/Serial Clock (I2C)	3
D24	OSC (PWDN)		
E1	AD1	Address 1	
E2	AD5	Address 5	
E3	GND	Ground	
E4	M66EN	Enable 66Mhz PCI-bus	
E5	GND	Ground	
E6	C/BE1#	Command, Byte Enable 1	
E7	SBO#	Snoop Backoff	1
E8	+5V	+5 VDC	
E9	IRDY#	Initatior Ready	1
E10	AD17	Address 17	
E11	GND	Ground	
E12	AD23	Address 23	
E13	C/BE3#	Command, Byte Enable 3	
E14	GND	Ground	
E15	AD30	Address 30	
E16	GNT1	Grant 1	
E17	+5V	+5 VDC	
E18	GNT4	Grant 4	
E19	X3	Reserved (3)	
E20	GND	Ground	
E21	INTC#	Interrupt C	1
E22	-12V	-12 VDC	
E23	+12V	+12 VDC	
E24	VBATT		

1 = Pullup resistor of 2,7 kW on the System Slot (CPU).
2 = Pullup resistor of 330 W on the System Slot (CPU). 3 = Pullup resistor of 4,7 kW, if not supported by the System Slot (CPU).

Module Bus Slot (Middle)

Pin	Name	Description	Note
A1	+3,3V	+3.3 VDC	
A2	AD2	Address 2	
A3	AD6	Address 6	
A4	GND	Ground	
A5	AD10	Address 10	
A6	AD13	Address 13	
A7	GND	Ground	
A8	SDONE	Snoop Done	1
A9	GND	Ground	
A10	FRAME#	Indicate Address or Data phase	1
A11	AD18	Address 18	
A12	GND	Ground	
A13	+5V	+5 VDC	
A14	AD24	Address 24	
A15	AD27	Address 27	

A16	GND	Ground	
A17	REQ2	Request 2	1
A18	CLKM		
A19	CLK1	33 or 66 MHz Clock	
A20	CLK2		
A21	GND	Ground	
A22	CLK3		
A23	CLK4		
A24	+3,3V	+3.3 VDC	
B1	REQ64#	Request 64 ???	1
B2	AD3	Address 3	
B3	+5V	+5 VDC	
B4	AD8	Address 8	
B5	+3,3V	+3.3 VDC	
B6	AD14	Address 14	
B7	PAR	Parity	
B8	+3,3V	+3.3 VDC	
B9	STOP#	Stop	1
B10	C/BE2#	Command, Byte Enable 2	
B11	V(I/O)	+3.3 or +5 VDC	
B12	AD21	Address 21	
B13	+3,3V	+3.3 VDC	
B14	V(I/O)	+3.3 or +5 VDC	
B15	AD28	Address 28	
B16	AD31	Address 31	
B17	+3,3V	+3.3 VDC	
B18	GNT3	Grant 3	
B19	RST#	Reset	
B20	NMI#	Non Maskable Interrupt	
B21	X6	Reserved (6)	
B22	+5V	+5 VDC	:
B23	RSTIN#		
B24	USB+	Universal Serial Bus (USB)(+)	
C1	ACK64#	Acknowledge 64 ???	1
C2	GND	Ground	
C3	AD7	Address 7	
C4	AD9	Address 9	
C5	AD11	Address 11	
C6	GND	Ground	
C7	SERR#	System Error	1
C8	PERR#	Parity Error	1
C9	DEVSEL#	Device Select	1
C10	GND	Ground	
C11	AD19	Address 19	
C12	AD22	Address 22	
C13	GND	Ground	
C14	AD25	Address 25	
C15	GND	Ground	
C16	X1	Reserved (1)	
C17	GNT2	Grant 2	
C18	REQ4	Request 4	1
C19	SLEEP#/SDAT	Sleep/Serial Data (I2C)	
C20	X4	Reserved (4)	
C21	INTD#	Interrupt D	1
C22	INTB#	Interrupt B	1
C23	+5V	+5 VDC	

C24	USB-	Universal Serial Bus (USB)(-)	
D1	AD0	Address 0	
D2	AD4	Address 4	
D3	C/BE0#	Command, Byte Enable 0	
D4	+3,3V	+3.3 VDC	
D5	AD12	Address 12	
D6	AD15	Address 15	
D7	V(I/O)	+3.3 or +5 VDC	
D8	LOCK#	Resource Lock	1
D9	TRDY#	Test Logic Ready	1
D10	AD16	Address 16	
D11	AD20	Address 20	
D12	+5V	+5 VDC	
D13	+5V	+5 VDC	
D14	AD26	Address 26	
D15	AD29	Address 29	
D16	REQ1	Request 1	1
D17	REQ3	Request 3	1
D18	V(I/O)	+3.3 or +5 VDC	
D19	X2	Reserved (2)	
D20	X5	Reserved (5)	
D21	+3,3V	+3.3 VDC	
D22	INTA#	Interrupt A	1
D23	ICPEN#/SCLK	ICPEN/Serial Clock (I2C)	3
D24	OSC (PWDN)		
E1	AD1	Address 1	
E2	AD5	Address 5	
E3	GND	Ground	
E4	M66EN	Enable 66Mhz PCI-bus	
E5	GND	Ground	
E6	C/BE1#	Command, Byte Enable 1	
E7	SBO#	Snoop Backoff	1
E8	+5V	+5 VDC	
E9	IRDY#	Initatior Ready	1
E10	AD17	Address 17	
E11	GND	Ground	
E12	AD23	Address 23	
E13	C/BE3#	Command, Byte Enable 3	
E14	GND	Ground	
E15	AD30	Address 30	
E16	GNT1	Grant 1	
E17	+5V	+5 VDC	
E18	GNT4	Grant 4	
E19	X3	Reserved (3)	
E20	GND	Ground	
E21	INTC#	Interrupt C	1
E22	-12V	-12 VDC	
E23	+12V	+12 VDC	
E24	VBATT		

1 = Pullup resistor of 2,7 kW on the System Slot (CPU).

Card Slot (Middle)

Pin	Name	Description	Note
A1	+3,3V	+3.3 VDC	
A2	AD2	Address 2	

A3	AD6	Address 6	
A4	GND	Ground	
A5	AD10	Address 10	
A6	AD13	Address 13	
A7	GND	Ground	
A8	SDONE	Snoop Done	1
A9	GND	Ground	
A10	FRAME#	Indicate Address or Data phase	1
A11	AD18	Address 18	
A12	GND	Ground	
A13	+5V	+5 VDC	
A14	AD24	Address 24	
A15	AD27	Address 27	
A16	GND	Ground	
A17	IDSEL0	IDSEL0	1
A18	GND	Ground	
A19	CLK1	33 or 66 MHz Clock	
A20	GND	Ground	
A21	GND	Ground	
A22	GND	Ground	
A23	GND	Ground	
A24	+3,3V	+3.3 VDC	
B1	REQ64#	Request 64 ???	1
B2	AD3	Address 3	
B3	+5V	+5 VDC	
B4	AD8	Address 8	
B5	+3,3V	+3.3 VDC	
B6	AD14	Address 14	
B7	PAR	Parity	
B8	+3,3V	+3.3 VDC	
B9	STOP#	Stop	1
B10	C/BE2#	Command, Byte Enable 2	
B11	V(I/O)	+3.3 or +5 VDC	
B12	AD21	Address 21	
B13	+3,3V	+3.3 VDC	
B14	V(I/O)	+3.3 or +5 VDC	
B15	AD28	Address 28	
B16	AD31	Address 31	
B17	+3,3V	+3.3 VDC	
B18	GND	Ground	
B19	RST#	Reset	
B20	NMI#	Non Maskable Interrupt	
B21	X6	Reserved (6)	
B22	+5V	+5 VDC	:
B23	RSTIN#		
B24	USB+	Universal Serial Bus (USB)(+)	
C1	ACK64#	Acknowledge 64 ???	1
C2	GND	Ground	
C3	AD7	Address 7	
C4	AD9	Address 9	
C5	AD11	Address 11	
C6	GND	Ground	
C7	SERR#	System Error	1
C8	PERR#	Parity Error	1
C9	DEVSEL#	Device Select	1
C10	GND	Ground	

C11	AD19	Address 19	
C12	AD22	Address 22	
C13	GND	Ground	
C14	AD25	Address 25	
C15	GND	Ground	
C16	X1	Reserved (1)	
C17	IDSEL1	Initialization Device Select 1	
C18	GND	Ground	
C19	SLEEP#/SDAT	Sleep/Serial Data (I2C)	
C20	X4	Reserved (4)	
C21	INTD#	Interrupt D	1
C22	INTB#	Interrupt B	1
C23	+5V	+5 VDC	
C24	USB-	Universal Serial Bus (USB)(-)	
D1	AD0	Address 0	
D2	AD4	Address 4	
D3	C/BE0#	Command, Byte Enable 0	
D4	+3,3V	+3.3 VDC	
D5	AD12	Address 12	
D6	AD15	Address 15	
D7	V(I/O)	+3.3 or +5 VDC	
D8	LOCK#	Resource Lock	1
D9	TRDY#	Test Logic Ready	1
D10	AD16	Address 16	
D11	AD20	Address 20	
D12	+5V	+5 VDC	
D13	+5V	+5 VDC	
D14	AD26	Address 26	
D15	AD29	Address 29	
D16	REQ1	Request 1	1
D17	IDSEL2	Initialization Device Select 2	
D18	V(I/O)	+3.3 or +5 VDC	
D19	X2	Reserved (2)	
D20	X5	Reserved (5)	
D21	+3,3V	+3.3 VDC	
D22	INTA#	Interrupt A	1
D23	ICPEN#/SCLK	ICPEN/Serial Clock (I2C)	3
D24	OSC (PWDN)		
E1	AD1	Address 1	
E2	AD5	Address 5	
E3	GND	Ground	
E4	M66EN	Enable 66Mhz PCI-bus	
E5	GND	Ground	
E6	C/BE1#	Command, Byte Enable 1	
E7	SBO#	Snoop Backoff	1
E8	+5V	+5 VDC	
E9	IRDY#	Initatior Ready	1
E10	AD17	Address 17	
E11	GND	Ground	
E12	AD23	Address 23	
E13	C/BE3#	Command, Byte Enable 3	
E14	GND	Ground	
E15	AD30	Address 30	
E16	GNT1	Grant 1	
E17	+5V	+5 VDC	
E18	GNT4	Grant 4	

E19	X3	Reserved (3)	
E20	GND	Ground	
E21	INTC#	Interrupt C	1
E22	-12V	-12 VDC	
E23	+12V	+12 VDC	
E24	VBATT		

1 = Pullup resistor of 2,7 kW on the System Slot (CPU).

64-bit PCI (Top)

Pin	Name	Description	Note
A1	GND	Ground	
A2	X10	Reserved (10)	
A3	AD35	Address 35	2
A4	AD38	Address 38	2
A5	AD42	Address 42	2
A6	V(I/O)	+3.3 or +5 VDC	
A7	V(I/O)	+3.3 or +5 VDC	
A8	AD52	Address 52	2
A9	AD56	Address 56	2
A10	AD60	Address 60	2
A11	AD63	Address 63	2
A12	GND	Ground	
B1	X7	Reserved (7)	
B2	GND	Ground	
B3	AD36	Address 36	2
B4	AD39	Address 39	2
B5	AD43	Address 43	2
B6	AD46	Address 46	2
B7	AD49	Address 49	2
B8	AD53	Address 53	2
B9	AD57	Address 57	2
B10	AD61	Address 61	2
B11	GND	Ground	
B12	C/BE6#	Command, Byte Enable 6	2
C1	X8	Reserved (8)	
C2	AD32	Address 32	2
C3	GND	Ground	
C4	AD40	Address 40	2
C5	AD44	Address 44	2
C6	GND	Ground	
C7	GND	Ground	
C8	AD54	Address 54	2
C9	AD58	Address 58	2
C10	GND	Ground	
C11	PAR64	Parity 64 ???	2
C12	C/BE7#	Command, Byte Enable 7	2
D1	X9	Reserved (9)	
D2	AD33	Address 33	2
D3	AD37	Address 37	2
D4	GND	Ground	
D5	AD45	Address 45	2
D6	AD47	Address 47	2
D7	AD50	Address 50	2
D8	AD55	Address 55	2
D9	GND	Ground	

D10	AD62	Address 62	2
D11	C/BE4#	Command, Byte Enable 4	2
D12	X11	Reserved (11)	
E1	GND	Ground	
E2	AD34	Address 34	2
E3	V(I/O)	+3.3 or +5 VDC	
E4	AD41	Address 41	2
E5	GND	Ground	
E6	AD48	Address 48	2
E7	AD51	Address 51	2
E8	GND	Ground	
E9	AD59	Address 59	2
E10	V(I/O)	+3.3 or +5 VDC	
E11	C/BE5#	Command, Byte Enable 5	2
E12	X12	Reserved (12)	

2 = Pullup resistor of 2,7 kW (5V bus system) or 8,2 kW (3,3V bus system) on the backplane.

ISA96/AT96 (Bottom)

Pin	Name	Description	Note
A1	RSTDRV		
A2	IRQ9	Interrupt 9	
A3	SD11	Data 11	
A4	SD9	Data 9	
A5	IOCHRDY		1
A6	IOW#	I/O Write	
A7	SA15	Address 15	
A8	CLK	Clock	
A9	SA10	Address 10	
A10	SA7	Address 7	
A11	T/C		
A12	SA2	Address 2	
B1	SD15	Data 15	
B2	SD13	Data 13	
B3	SD3	Data 3	
B4	SD1	Data 1	
B5	SMEMW#	System Memory Write	
B6	SA18	Address 18	
B7	SA14	Address 14	
B8	DACK6#	DMA Acknowledge 6	
B9	SA9	Address 9	
B10	IRQ3	Interrupt 3	
B11	IOCS16#	I/O 16-bit chip select	1
B12	SA1	Address 1	
C1	SD7	Data 7	
C2	SD5	Data 5	
C3	SD10	Data 10	
C4	SD8	Data 8	
C5	AEN	Address Enable	
C6	IOR#	I/O Read	
C7	SA13	Address 13	
C8	SA11	Address 11	
C9	IRQ5	Interrupt 5	
C10	SA6	Address 6	
C11	SA4	Address 4	

C12	IRQ11	Interrupt 11	
D1	SD14	Data 14	
D2	SD12	Data 12	
D3	SD2	Data 2	
D4	SD0	Data 0	
D5	SMEMR#	System Memory Read	
D6	SA17	Address 17	
D7	REF#		
D8	IRQ7	Interrupt 7	
D9	SA8	Address 8	
D10	MCS16#		1
D11	BALE		
D12	SA0	Address 0	
E1	SD6	Data 6	
E2	SD4	Data 4	
E3	0WS		1
E4	SBHE#		
E5	SA19	Address 19	
E6	SA16	Address 16	
E7	SA12	Address 12	
E8	DRQ6	DMA Request 6	
E9	IRQ4	Interrupt 4	
E10	SA5	Address 5	
E11	SA3	Address 3	
E12	IRQ10	Interrupt 10	

1 = Pullup resistor must be integrated into the System Slot (CPU).

VMEbus (Bottom)

Pin	Name	Description
A1	D0	Data 0
A2	D2	Data 2
A3	D12	Data 12
A4	D7	Data 7
A5	DS1#	
A6	BR3#	
A7	AM1	
A8	AM3	
A9	IACKOUT#	
A10	A14	Address 14
A11	A12	Address 12
A12	A10	Address 10
B1	BBSY#	
B2	D10	Data 10
B3	D5	Data 5
B4	D15	Data 15
B5	SYSRES#	
B6	A23	Address 23
B7	A21	Address 21
B8	A19	Address 19
B9	A16	Address 16
B10	A6	Address 6
B11	A4	Address 4
B12	A2	Address 2
C1	D8	Data 8
C2	D3	Data 3

C3	D13	Data 13
C4	SYSCLK	
C5	DS0#	
C6	DTACK#	
C7	AS#	
C8	IACK#	
C9	AM4	
C10	A13	Address 13
C11	A11	Address 11
C12	A9	Address 9
D1	D1	Data 1
D2	D11	Data 11
D3	D6	Data 6
D4	BG3OUT#	
D5	WR#	Write
D6	AM0	
D7	AM2	
D8	A18	Address 18
D9	A15	Address 15
D10	A5	Address 5
D11	A3	Address 3
D12	A1	Address 1
E1	D9	Data 9
E2	D4	Data 4
E3	D14	Data 14
E4	BERR#	Bus Error
E5	AM5	
E6	A22	Address 22
E7	A20	Address 20
E8	A17	Address 17
E9	A7	Address 7
E10	IRQ5#	Interrupt 5
E11	IRQ3#	Interrupt 3
E12	A8	Address 8

ECB (Bottom)

Pin	Name	Description
A1	D5	Data 5
A2	D2	Data 2
A3	A4	Data 4
A4	A7	Address 7
A5	BAI	
A6	2F	
A7	A10	Address 10
A8	INT#	
A9	VCMOS	
A10	PWRCLR#	
A11	A13	Address 13
A12	RESET#	Reset
B1	D0	Data 0
B2	D4	Data 4
B3	A1	Address 1
B4	WAIT#	
B5	A17	Address 17
B6	IEO	

B7	n/c	Not connected
B8	DMARDY	
B9	RD#	Read
B10	IORQ#	
B11	?	
B12	n/c	Not connected
C1	D6	Data 6
C2	A0	Address 0
C3	A5	Address 5
C4	A16	Address 16
C5	A18	Address 18
C6	BAO	
C7	M1#	
C8	WR#	
C9	n	
C10	A12	Address 12
C11	A9	Address 9
C12	n/c	Not connected
D1	D7	Data 7
D2	A2	Address 2
D3	A8	Address 8
D4	BUSRQ#	
D5	A19	Address 19
D6	A11	Address 11
D7	NMI#	Non Maskable Interrupt
D8	PF	
D9	HALT#	
D10	RFSH#	
D11	MRQ#	
D12	n/c	Not connected
E1	D3	Data 3
E2	A3	Address 3
E3	A6	Address 6
E4	IEI	
E5	D1	Data 1
E6	A14	Address 14
E7	n/c	Not connected
E8	n/c	Not connected
E9	DESLCT#	
E10	A15	Address 15
E11	BUSAK#	
E12	n/c	Not connected

SMP16 (Bottom)

Pin	Name	Description
A1	NMI#	Non Maskable Interrupt
A2	IRQ0#	Interrupt 0
A3	D11	Data 11
A4	D9	Data 9
A5	RDYIN	
A6	IOW#	
A7	A15	Address 15
A8	CLK	
A9	A10	Address 10
A10	A7	Address 7

A11	TC/EOP#	
A12	A2	Address 2
B1	D15	Data 15
B2	D13	Data 13
B3	D3	Data 3
B4	D1	Data 1
B5	MEMW#	
B6	A18	Address 18
B7	A14	Address 14
B8	DACKx#	
B9	A9	Address 9
B10	IRQ3#	Interrupt 3
B11	IOCS16#	
B12	A1	Address 1
C1	D7	Data 7
C2	D5	Data 5
C3	D10	Data 10
C4	D8	Data 8
C5	BUSEN	
C6	IOR#	
C7	A13	Address 13
C8	A11	Address 11
C9	IRQ1#	Interrupt 1
C10	A6	Address 6
C11	A4	Address 4
C12	IRQ4#	Interrupt 4
D1	D14	Data 14
D2	D12	Data 12
D3	D2	Data 2
D4	D0	Data 0
D5	MEMR#	
D6	A17	Address 17
D7	INTA#	
D8	INT#	
D9	A8	Address 8
D10	MECS16#	
D11	ALE	
D12	A0	Address 0
E1	D6	Data 6
E2	D4	Data 4
E3	MMIO#	
E4	BHEN	
E5	A19	Address 19
E6	A16	Address 16
E7	A12	Address 12
E8	DRQx#	
E9	IRQ2#	Interrupt 2
E10	A5	Address 5
E11	A3	Address 3
E12	IRQ5#	Interrupt 5

Floppy/EIDE (Bottom)

Pin	Name	Description
A1	FDSEL1	Floppy Select 1
A2	FDSEL0	Floppy Select 0

A3	FDME1	Floppy ?
A4	DIR	Floppy Direction
A5	STEP	Floppy Step
A6	WRDATA	Floppy Write Data
A7	WE	Floppy Write?
A8	TRK0	Floppy Track 0
A9	WP	Floppy Write?
A10	RDDATA	Floppy ?
A11	HDSEL	Floppy HD Select
A12	DSKCHG	Floppy DiskChange
B1	DRVDEN1	?
B2	DRVDEN0	?
B3	IDECS3P#	IDE ?
B4	IDEA2	IDE ?
B5	IDEIRQS	IDE ?
B6	IDEPUS	IDE ?
B7	IDEDRQP	IDE ?
B8	IDED14	IDE Data 14
B9	IDED8	IDE Data 8
B10	IDED6	IDE Data 6
B11	IDED11	IDE Data 11
B12	IDED3	IDE Data 3
C1	FDME0	Floppy Me?
C2	INDX	Floppy Index
C3	IDECS3S#	IDE ?
C4	IDEA0	IDE ?
C5	IDEDAKS#	IDE ?
C6	IDEIOR#	IDE ?
C7	IDEDRQS	IDE ?
C8	IDED1	IDE Data 1
C9	#IDERST	IDE ?
C10	IDED10	IDE Data 10
C11	IDED4	IDE Data 4
C12	IDED2	IDE Data 2
D1	IDELEDS#	IDE LED ?
D2	IDELEDP#	IDE LED ?
D3	IDECS1S#	IDE ?
D4	IDEIRQP	IDE ?
D5	IDEPUP	IDE Pull Up ?
D6	IDEIOW#	IDE ?
D7	IDED15	IDE Data 15
D8	IDED13	IDE Data 13
D9	IDED7	IDE Data 7
D10	GND	Ground
D11	GND	Ground
D12	GND	Ground
E1	GND	Ground
E2	GND	Ground
E3	IDECS1P#	IDE ?
E4	IDEA1	IDE ?
E5	IDEDAKP#	IDE ?
E6	IDEIORDY	IDE ?
E7	IDED0	IDE Data 0
E8	IDED12	IDE Data 12
E9	IDED9	IDE Data 9
E10	IDED5	IDE Data 5

E11	GND	Ground
E12	GND	Ground

SCSI (Bottom)

Pin	Name	Description
A1	TERM	
A2	GND	Ground
A3	I/O#	
A4	REQ#	
A5	ATN#	
A6	D8	Data 8
A7	D9	Data 9
A8	D10	Data 10
A9	D2	Data 2
A10	D4	Data 4
A11	DP0	
A12	GND	Ground
B1	TERM	
B2	GND	Ground
B3	GND	Ground
B4	GND	Ground
B5	GND	Ground
B6	GND	Ground
B7	GND	Ground
B8	GND	Ground
B9	GND	Ground
B10	GND	Ground
B11	GND	Ground
B12	GND	Ground
C1	TERM	
C2	GND	Ground
C3	C/D#	
C4	MSG#	
C5	ACK#	
C6	D12	Data 12
C7	DP1	Data P1
C8	D13	Data 13
C9	D1	Data 1
C10	D5	Data 5
C11	D7	Data 7
C12	GND	Ground
D1	TERM	
D2	GND	Ground
D3	GND	Ground
D4	GND	Ground
D5	GND	Ground
D6	GND	Ground
D7	GND	Ground
D8	GND	Ground
D9	GND	Ground
D10	GND	Ground
D11	GND	Ground
D12	GND	Ground
E1	TERM	
E2	GND	Ground

E3	SEL#	
E4	RST#	
E5	BSY#	
E6	D14	Data 14
E7	D15	Data 15
E8	D11	Data 11
E9	D0	Data 0
E10	D3	Data 3
E11	D6	Data 6
E12	GND	Ground

Contributor: Joakim Ogren

Sources:IndustrialPCI page at Standard Industrial PC Systems's (SIPS) homepage

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.sips.com/ipci.htm
Open this address in your WWW browser.

This is the URL for the WWW page:
http://www.sips.com
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SmallPCI Connector

NEW
NEW
NEW

SmallPCI (SPCI)

PCI=Peripheral Component Interconnect.
SmallPCI is a a version of PCI adapted for small computers and PDAs.

NEW (At the motherboard)

NEW (At the device)

UNKNOWN CONNECTOR at the motherboard.
UNKNOWN CONNECTOR at the device.

I don't have any technical information about SmallPCI at the moment. If you have any information of value please send it to me.

The specifications can be obtained from:

PCI Special Interrest Group
2575 NE Kathryn St. #17
Hillsboro, OR 97124
Phone: 1-800-433-5177
Fax: 1-503-693-8344

Contributor: Joakim Ogren

Source:?

Info: SmallPCI overview at PCI Speacial Interrest Group's homepage

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.pcisig.com/current/smallpci.html
Open this address in your WWW browser.

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http://www.pcisig.com
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Miniature Card Connector

NEW
NEW
NEW

Miniature Card

Developed by Intel.
Miniature Card is a memory-only expansion card.

NEW (At the device)

NEW (At the card)

UNKNOWN CONNECTOR at the device.
UNKNOWN CONNECTOR at the card.

Pin	Name	Description	Dir
1	A18	Address Bus	NEW
2	A16	Address Bus	NEW
3	A14	Address Bus	NEW
4	Vccr	Voltage Refresh	NEW
5	CEH#	Card Enable High Byte	NEW
6	A11	Address Bus	NEW
7	A9	Address Bus	NEW
8	A8	Address Bus	NEW
9	A6	Address Bus	NEW
10	A5	Address Bus	NEW
11	A3	Address Bus	NEW
12	A2	Address Bus	NEW
13	A0	Address Bus	NEW
14	RAS#	Row Address Strobe	NEW
15	A24	Address Bus	NEW
16	A23	Address Bus	NEW
17	A22	Address Bus	NEW
18	OE#	Output Enable	NEW
19	D15	Data Bus	NEW
20	D13	Data Bus	NEW
21	D12	Data Bus	NEW
22	D10	Data Bus	NEW
23	D9	Data Bus	NEW
24	D0	Data Bus	NEW
25	D2	Data Bus	NEW
26	D4	Data Bus	NEW
27	RFU	Reserved for future use	
28	D7	Data Bus	NEW
29	SDA	Serial Data and Address	NEW
30	SCL	Serial Clock	NEW
31	A19	Address Bus	NEW
32	A17	Address Bus	NEW
33	A15	Address Bus	NEW
34	A13	Address Bus	NEW
35	A12	Address Bus	NEW
36	RESET#	Reset	NEW
37	A10	Address Bus	NEW
38	VS1#	Voltage Sense 1	NEW
39	A7	Address Bus	NEW

40	BS8#	Bus Size 8	NEW
41	A4	Address Bus	NEW
42	CEL#	Card Enable Low Byte	NEW
43	A1	Address Bus	NEW
44	CASL#	Column Address Strobe Low Byte	NEW
45	CASH#	Column Address Strobe High Byte	NEW
46	CD#	Card Detect	NEW
47	A21	Address Bus	NEW
48	BUSY#	Ready/Busy	NEW
49	WE#	Write Enable	NEW
50	D14	Data Bus	NEW
51	RFU	Reserved for future use	
52	D11	Data Bus	NEW
53	VS2#	Voltage Sense 2	NEW
54	D8	Data Bus	NEW
55	D1	Data Bus	NEW
56	D3	Data Bus	NEW
57	D5	Data Bus	NEW
58	D6	Data Bus	NEW
59	RFU	Reserved for future use	
60	A20	Address Bus	NEW

The following three is separate:

Name	**Description**	**Dir**
GND	Ground	
VCC	Power	
CINS#	Card Insertion	NEW

Note: Direction is card relative device.

Contributor: Joakim Ogren

Source:Minicature Card v1.1 spec at Miniature Card Implementers Forum's homepage

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.mcif.org/spec.html
Open this address in your WWW browser.

Miniature Card (Technical)

This section is currently based soly on the Miniature Card specification v1.1.

Signal Descriptions:

A0-A24

Address A0 to A24 are the address bus lines that can address up to 32 Mwords (64 MBytes). The Miniature Card specification does not require the Miniature Card to decode the upper address lines. A 2 Mbyte Miniature Card that does not decode the upper address lines would repeat its address space every 2 Mbytes. Address 0h would access the same physical location as 200000h, 400000h, 600000h, etc.

D0-D15

Data lines D0 through D15 constitute the data bus. The data bus is composed of two bytes, the low byte D[7:0] and the high byte D[15:8].

OE#

OE# indicates that the current bus cycle is a read cycle.

WE#

WE# indicates that the current bus cycle is a write cycle.

VS1#

Voltage Sense 1 signal. The card grounds this signal to indicate it can operate at 3.3 Volts. This signal must either be connected to card GND or left open.

VS2#

Voltage Sense 2 signal. The card grounds this signal to indicate it can operate at x.x Volts (the value to be determined at a later date). This signal must either be connected to card GND or left open.

CEL#

CEL# enables the low byte of the data bus (D[7:0]) on the card. This signal is not used in DRAM cards.

CEH#

CEH# enables the high byte of the data bus (D[15:8]) on the card. This signal is not used in DRAM cards.

RAS#

RAS# strobes in the row address for DRAM cards.

CASL#

CASL# strobes in the low byte column address for DRAM cards.

CASH#

CASH# strobes in the high byte column address for DRAM cards.

RESET#

RESET# controls card initialization. When RESET# transitions from a low state to a high state, the Miniature Card must reset to a predetermined state.

BUSY#

BUSY# is a signal generated by the card to indicate the status of operations within the Miniature Card. When BUSY# is high, the Miniature Card is ready to accept the next command from the host. When BUSY# is low, the Miniature Card is busy and unable to accept some data operations from the host. For example, in Flash Miniature Cards the BUSY# signal is tied to the components RY/BY# signal. However, ROM Miniature Cards would always drive BUSY# high since the host will always be able to read from a ROM Miniature Card.

Vccr

Vccr provides a low current (refresh) voltage supply. Vccr is a feature used by DRAM Miniature Cards to "self-refresh" during "sleep" mode.

SDA

I2C: Serial Data/Address.

SCL

I2C: Serial Clock are used to read the attribute information structure (AIS) from the serial EEPROM in a DRAM card.

CD#

CD# is a grounded interface signal. After a Miniature Card has been inserted, CD# will be forced low. The card detect signal is located in the center of the second row of interface signals, and should be one of the last interface signals to connect to the host. Do not confuse CD# with CINS#. CINS# is an early card detect that is one of the first signals to connect to the host.

BS8#

BS8# is a signal driven by the host to indicate if the data bus is x8 or x16. An 8-bit host must drive BS8# low and tie the high byte data bus D[15:8] to the low byte data bus D[7:0]. A 16-bit host must drive this signal high.

GND

Ground

Vcc

Vcc is used to supply power to the card.

CINS#

CINS# is a grounded signal on the front of the Miniature Card that can be used for early detection of a card insertion. CINS# makes contact on the host when the front of the card is inserted into the socket, before the interface signals connect.

Contributor: Joakim Ogren

Source:Minicature Card v1.1 spec at Miniature Card Implementers Forum's homepage

Please send any comments to Joakim Ogren.

Zorro II Connector

NEW
NEW
NEW

Zorro II

NEW (At the A2000)
86 PIN EDGE CONNECTOR at the A2000.
NOTE: All of my X's suddenly disappeared. I have now put them back again. I hope the table is correct. Please contact me if not. I don't remember where I found this information.

Pin	A500	A1000	A2000	A2000B	Name	Description
1	X	X	X	X	GND	Ground
2	X	X	X	X	GND	Ground
3	X	X	X	X	GND	Ground
4	X	X	X	X	GND	Ground
5	X	X	X	X	+5V	+5 Volts DC
6	X	X	X	X	+5V	+5 Volts DC
7	X	X	X	X	n/c	
8	X	X	X	X	-5V	-5 Volts DC
9	X	X			n/c	
			X	X	28CLOCK	28MHz Clock
10	X	X	X	X	+12V	+12 Volts DC
11	X	X			n/c	
			X	X	/COPCFG	Configuration Out
12	X	X	X	X	CONFIG IN, Grounded	
13	X	X	X	X	GND	Ground
14	X	X	X	X	/C3	C3 Clock
15	X	X	X	X	CDAC	Clock
16	X	X	X	X	/C1	C1 Clock
17	X	X	X	X	/OVR	
18	X	X	X	X	RDY	Ready
19	X	X	X	X	/INT2	Interrupt 2
20	X	X			/PALOPE	
			X		n/c	
				X	/BOSS	
21	X	X	X	X	A5	Address 5
22	X	X	X	X	/INT6	Interrupt 6
23	X	X	X	X	A6	Address 6
24	X	X	X	X	A4	Address 4
25	X	X	X	X	GND	Ground
26	X	X	X	X	A3	Address 3
27	X	X	X	X	A2	Address 2
28	X	X	X	X	A7	Address 7
29	X	X	X	X	A1	Address 1
30	X	X	X	X	A8	Address 8
31	X	X	X	X	FC0	Processor status 0
32	X	X	X	X	A9	Address 9
33	X	X	X	X	FC1	Processor status 1
34	X	X	X	X	A10	Address 10
35	X	X	X	X	FC2	Processor status 2
36	X	X	X	X	A11	Address 11
37	X	X	X	X	GND	Ground
38	X	X	X	X	A12	Address 12

39	X	X	X	X	A13	Address 13
40	X	X	X	X	/IPL0	
41	X	X	X	X	A14	Address 14
42	X	X	X	X	/IPL1	
43	X	X	X	X	A15	Address 15
44	X	X	X	X	/IPL2	
45	X	X	X	X	A16	Address 16
46	X	X	X	X	/BEER	Bus Error
47	X	X	X	X	A17	Address
48	X	X	X	X	/VPA	
49	X	X	X	X	GND	Ground
50	X	X	X	X	ECLK	E Clock
51	X	X	X	X	/VMA	
52	X	X	X	X	A18	Address 18
53	X	X	X	X	RST	Reset
54	X	X	X	X	A19	Address 19
55	X	X	X	X	/HLT	Halt
56	X	X	X	X	A20	Address 20
57	X	X	X	X	A22	Address 22
58	X	X	X	X	A21	Address 21
59	X	X	X	X	A23	Address 23
60	X	X			/BR	
			X	X	/CBR	
61	X	X	X	X	GND	Ground
62	X	X	X	X	/BGACK	
63	X	X	X	X	D15	Data 15
64	X	X			/BG	
			X	X	/CBG	
65	X	X	X	X	D14	Data 14
66	X	X	X	X	/DTACK	
67	X	X	X	X	D13	Data 13
68	X	X	X	X	R/W	Read/Write
69	X	X	X	X	D12	Data 12
70	X	X	X	X	/LDS	
71	X	X	X	X	D11	Data 11
72	X	X	X	X	/UDS	
73	X	X	X	X	GND	Ground
74	X	X	X	X	/AS	
75	X	X	X	X	D0	Data 0
76	X	X	X	X	D10	Data 10
77	X	X	X	X	D1	Data 1
78	X	X	X	X	D9	Data 9
79	X	X	X	X	D2	Data 2
80	X	X	X	X	D8	Data 8
81	X	X	X	X	D3	Data 3
82	X	X	X	X	D7	Data 7
83	X	X	X	X	D4	Data 4
84	X	X	X	X	D6	Data 6
85	X	X	X	X	GND	Ground
86	X	X	X	X	D5	Data 5

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Zorro II/III Connector

NEW
NEW
NEW

Zorro II/III

NEW (At the computer)
100 PIN EDGE CONNECTOR at the computer.

Pin	Physical Name	Zorro II Name	Zorro III Address Phase	Zorro III Data Phase
1	Ground	Ground	Ground	Ground
2	Ground	Ground	Ground	Ground
3	Ground	Ground	Ground	Ground
4	Ground	Ground	Ground	Ground
5	+5VDC	+5VDC	+5VDC	+5VDC
6	+5VDC	+5VDC	+5VDC	+5VDC
7	/OWN	/OWN	/OWN	/OWN
8	-5VDC	-5VDC	-5VDC	-5VDC
9	/SLAVEn	/SLAVEn	/SLAVEn	/SLAVEn
10	+12VDC	+12VDC	+12VDC	+12VDC
11	/CFGOUTn	/CFGOUTn	/CFGOUTn	/CFGOUTn
12	/CFGINn	/CFGINn	/CFGINn	/CFGINn
13	Ground	Ground	Ground	Ground
14	/C3	/C3 Clock	/C3 Clock	/C3 Clock
15	CDAC	CDAC Clock	CDAC Clock	CDAC Clock
16	/C1	/C1 Clock	/C1 Clock	/C1 Clock
17	/CINH	/OVR	/CINH	/CINH
18	/MTCR	XRDY	/MTCR	/MTCR
19	/INT2	/INT2	/INT2	/INT2
20	-12VDC	-12VDC	-12VDC	-12VDC
21	A5	A5	A5	A5
22	/INT6	/INT6	/INT6	/INT6
23	A6	A6	A6	A6
24	A4	A4	A4	A4
25	Ground	Ground	Ground	Ground
26	A3	A3	A3	A3
27	A2	A2	A2	A2
28	A7	A7	A7	A7
29	/LOCK	A1	/LOCK	/LOCK
30	AD8	A8	A8	D0
31	FC0	FC0	FC0	FC0
32	AD9	A9	A9	D1
33	FC1	FC1	FC1	FC1
34	AD10	A10	A10	D2
35	FC2	FC2	FC2	FC2
36	AD11	A11	A11	D3
37	Ground	Ground	Ground	Ground
38	AD12	A12	A12	D4
39	AD13	A13	A13	D5
40	Reserved	(/EINT7)	Reserved	Reserved
41	AD14	A14	A14	D6
42	Reserved	(/EINT5)	Reserved	Reserved
43	AD15	A15	A15	D7
44	Reserved	(/EINT4)	Reserved	Reserved

45	AD16	A16	A16	D8
46	/BERR	/BERR	/BERR	/BERR
47	AD17	A17	A17	D9
48	/MTACK	(/VPA)	/MTACK	/MTACK
49	Ground	Ground	Ground	Ground
50	E Clock	E Clock	E Clock	E Clock
51	/DS0	(/VMA)	/DS0	/DS0
52	AD18	A18	A18	D10
53	/RESET	/RST	/RESET	/RESET
54	AD19	A19	A19	D11
55	/HLT	/HLT	/HLT	/HLT
56	AD20	A20	A20	D12
57	AD22	A22	A22	D14
58	AD21	A21	A21	D13
59	AD23	A23	A23	D15
60	/BRn	/BRn	/BRn	/BRn
61	Ground	Ground	Ground	Ground
62	/BGACK	/BGACK	/BGACK	/BGACK
63	AD31	D15	A31	D31
64	/BGn	/BGn	/BGn	/BGn
65	AD30	D14	A30	D30
66	/DTACK	/DTACK	/DTACK	/DTACK
67	AD29	D13	A29	D29
68	READ	READ	READ	READ
69	AD28	D12	A28	D28
70	/DS2	/LDS	/DS2	/DS2
71	AD27	D11	A27	D27
72	/DS3	/UDS	/DS3	/DS3
73	Ground	Ground	Ground	Ground
74	/CCS	/AS	/CCS	/CCS
75	SD0	D0	Reserved	D16
76	AD26	D10	A26	D26
77	SD1	D1	Reserved	D17
78	AD25	D9	A25	D25
79	SD2	D2	Reserved	D18
80	AD24	D8	A24	D24
81	SD3	D3	Reserved	D19
82	SD7	D7	Reserved	D23
83	SD4	D4	Reserved	D20
84	SD6	D6	Reserved	D22
85	Ground	Ground	Ground	Ground
86	SD5	D5	Reserved	D21
87	Ground	Ground	Ground	Ground
88	Ground	Ground	Ground	Ground
89	Ground	Ground	Ground	Ground
90	Ground	Ground	Ground	Ground
91	SenseZ3	Ground	SenseZ3	SenseZ3
92	7M	E7M	7M	7M
93	DOE	DOE	DOE	DOE
94	/IORST	/BUSRST	/IORST	/IORST
95	/BCLR	/GBG	/BCLR	/BCLR
96	Reserved	(/EINT1)	Reserved	Reserved
97	/FCS	No Connect	/FCS	/FCS
98	/DS1	No Connect	/DS1	/DS1
99	Ground	Ground	Ground	Ground
100	Ground	Ground	Ground	Ground

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

Amiga 1200 CPU-port Connector

NEW
NEW
NEW

Amiga 1200 CPU-port

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	n/c	Reserved
2	n/c	Reserved
3	n/c	Reserved
4	n/c	Reserved
5	n/c	Reserved
6	n/c	Reserved
7	n/c	Reserved
8	n/c	Reserved
9	GND	Ground
10	+5V	+5 Volts DC
11	A23	Address 23
12	A22	Address 22
13	A21	Address 21
14	A20	Address 20
15	A19	Address 19
16	A18	Address 18
17	A17	Address 17
18	A16	Address 16
19	GND	Ground
20	+5V	+5 Volts DC
21	A15	Address 15
22	A14	Address 14
23	A13	Address 13
24	A12	Address 12
25	A11	Address 11
26	A10	Address 10
27	A9	Address 9
28	A8	Address 8
29	GND	Ground
30	+5V	+5 Volts DC
31	A7	Address 7
32	A6	Address 6
33	A5	Address 5
34	A4	Address 4
35	A3	Address 3
36	A2	Address 2
37	A1	Address 1
38	A0	Address 0
39	GND	Ground
40	+5V	+5 Volts DC
41	D31	Data 31
42	D30	Data 30
43	D29	Data 29
44	D28	Data 28
45	D27	Data 27

46	D26	Data 26
47	D25	Data 25
48	D24	Data 24
49	GND	Ground
50	+5V	+5 Volts DC
51	D23	Data 23
52	D22	Data 22
53	D21	Data 21
54	D20	Data 20
55	D19	Data 19
56	D18	Data 18
57	D17	Data 17
58	D16	Data 16
59	GND	Ground
60	+5V	+5 Volts DC
61	D15	Data 15
62	D14	Data 14
63	D13	Data 13
64	D12	Data 12
65	D11	Data 11
66	D10	Data 10
67	D9	Data 9
68	D8	Data 8
69	GND	Ground
70	+5V	+5 Volts DC
71	D7	Data 7
72	D6	Data 6
73	D5	Data 5
74	D4	Data 4
75	D3	Data 3
76	D2	Data 2
77	D1	Data 1
78	D0	Data 0
79	GND	Ground
80	+5V	+5 Volts DC
81	/IPL2	
82	/IPL1	
83	/IPL0	
84	n/c	Reserved
85	/RST	Reset
86	/HLT	Halt
87	n/c	Reserved
88	n/c	Reserved
89	SIZE1	
90	SIZE0	
91	/AS	Address Strobe
92	/DS	Data Strobe
93	R/W	Read/Write
94	/BERR	Bus Error
95	n/c	Reserved
96	/AVEC	
97	/DSACK1	
98	/DSACK2	
99	CPUCKLA	
100	ECLOCK	EClock pulse
101	GND	Ground

102	+5V	+5 Volts DC
103	FC2	Processor Status 2
104	FC1	Processor Status 1
105	FC0	Processor Status 0
106	/RMC	
107	n/c	Reserved
108	n/c	Reserved
109	n/c	Reserved
110	n/c	Reserved
111	/BR	Slot specific Bus Arbitration
112	/BG	Slot specific Bus Arbitration
113	n/c	Reserved
114	/BOSS	
115	/FPUCS	FPU Chip select
116	/FPUSENSE	FPU Sense
117	CCKA	
118	/RESET	Reset
119	GND	Ground
120	+5V	+5 Volts DC
121	/NETCS	
122	/SPARECS	
123	/RTCCS	Realtime Clock Chip select
124	/FLASH	
125	/REG	
126	/CCENA	
127	/WAIT	
128	/KBRESET	Keyboard reset
129	/IORD	IO Read
130	/IOWR	IO Write
131	/OE	Output enable
132	/WE	
133	/OVR	/DTACK Override
134	XRDY	External Ready
135	/ZORRO	
136	/WIDE	
137	/INT2	Interrupt level 2
138	/INT6	Interrupt level 6
139	GND	Ground
140	+5V	+5 Volts DC
141	SYSTEM1	System1 Ground
142	SYSTEM0	System0 Ground
143	/xRxD	
144	/xTxD	
145	/CONFIG OUT	
146	AGND	Audio Ground
147	ALEFT	Audio Left
148	ARIGHT	Audio Right
149	+12V	+12 Volts DC
150	-12V	-12 Volts DC

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Amiga 1000 Ramex Connector

NEW
NEW
NEW

Amiga 1000 Ramex

NEW (At the computer)
60 PIN EDGE CONNECTOR (.156") at the computer.

Pin	Name	Description
1	GND	Ground
2	D15	Data 15
3	+5V	+5 Volts DC
4	D12	Data 12
5	GND	Ground
6	D11	Data 11
7	+5V	+5 Volts DC
8	D8	Data 8
9	GND	Ground
10	D7	Data 7
11	+5V	+5 Volts DC
12	D4	Data 4
13	GND	Ground
14	D3	Data 3
15	+5V	+5 Volts DC
16	D0	Data 0
17	GND	Ground
18	DRA4	
19	DRA5	
20	DRA6	
21	DRA7	
22	GND	Ground
23	/RAS	
24	GND	Ground
25	GND	Ground
26	/CASU0	
27	GND	Ground
28	/CASL0	
29	+5V	+5 Volts DC
30	+5V	+5 Volts DC
A	GND	Ground
B	D14	Data 14
C	+5V	+5 Volts DC
D	D13	Data 13
E	GND	Ground
F	D10	Data 10
H	+5V	+5 Volts DC
J	D9	Data 9
K	GND	Ground
L	D6	Data 6
M	+5V	+5 Volts DC
N	D5	Data 5
P	GND	Ground
R	D2	Data 2

S	+5V	+5 Volts DC
T	D1	Data 1
U	GND	Ground
V	DRA3	
W	DRA2	
X	DRA1	
Y	DRA0	
Z	GND	Ground
AA	/RRW	
BB	GND	Ground
CC	GND	Ground
DD	/CASU1	
EE	GND	Ground
FF	/CASL1	
HH	+5V	+5 Volts DC
JJ	+5V	+5 Volts DC

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Amiga Video Expansion Connector

NEW
NEW
NEW

Video Expansion (Amiga)

NEW (At the computer)
36+54 PIN EDGE CONNECTOR at the computer.

Pin	Name	Dir	Description
1	RGB16	NEW	Red Bit 0
2	RGB17	NEW	Red Bit 1
3	LINELF	NEW	Audio Line Out Left
4	LINERT	NEW	Audio Line Out Right
5	C28D	NEW	Pixel-Synchronous Clock
6	+5V	-	+5 Volts DC (1 A)
7	ARED	NEW	Analog Red
8	+5V	-	+5 Volts DC (1 A)
9	GND	-	Digital Ground
10	+12V	-	+12 Volts DC (40 mA)
11	AGREEN	NEW	Analog Green
12	GND	-	Digital Ground
13	GND	-	Digital Ground
14	/CSYNC	NEW	Composite Sync
15	ABLUE	NEW	Analog Blue
16	/XCLKEN	NEW	Genlock Clock Enable
17	GND	-	Digital Ground
18	BURST	NEW	Burst Gate
19	/C4	NEW	3.55/3.58 MHz Clock
20	GND	-	Digital Ground
21	GND	-	Digital Ground
22	/HSYNC	NEW	Horizontal Sync (47 Ohm)
23	RGB4	NEW	Blue Bit 4
24	GND	-	Digital Ground
25	RGB7	NEW	Blue Bit 7
26	/VSYNC	NEW	Vertical Sync (47 Ohm)
27	RGB15	NEW	Green Bit 7
28	BLANK	NEW	Video Blank
29	RGB23	NEW	Red 7
30	/PIXELSW	NEW	Genlock Overlay (47 Ohm)
31	-5V	-	-5 Volts DC
32	GND	-	Digital Ground
33	/XCLK	NEW	Genlock Clock
34	/C1	NEW	C1 Clock
35	+5V	-	+5 Volts DC (1 A)
36	PSTROBE	NEW	Printer Port Handshake
1	GND	-	Digital Ground
2	RGB20	NEW	Red Bit 4
3	RGB21	NEW	Red Bit 5
4	RGB22	NEW	Red Bit 6
5	GND	-	Digital Ground
6	RGB12	NEW	Green Bit 4
7	RGB13	NEW	Green Bit 5
8	RGB14	NEW	Green Bit 6

9	GND	-	Digital Ground
10	RGB5	NEW	Blue Bit 5
11	RGB6	NEW	Blue Bit 6
12	GND	-	Ground
13	SOG	NEW	Sync-On-Green Indicator
14	TBASE	NEW	50/60 Hz Software Clock Timebase
15	CDAC	NEW	7.09/7.16 MHz Clock
16	PPOUT	NEW	Printer Port Paper Out
17	/C3	NEW	3.55/3.58 MHz Clock
18	PBUSY	NEW	Printer Port Busy
19	/LPEN	NEW	Light Pen Input
20	/PACK	NEW	Printer Port Acknowledge Handshake
21	PSEL	NEW	Printer Port Select
22	GND	-	Digital Ground
23	PPD0	NEW	Printer Port Data Bit 0
24	PPD1	NEW	Printer Port Data Bit 1
25	PPD2	NEW	Printer Port Data Bit 2
26	PPD3	NEW	Printer Port Data Bit 3
27	PPD4	NEW	Printer Port Data Bit 4
28	PPD5	NEW	Printer Port Data Bit 5
29	PPD6	NEW	Printer Port Data Bit 6
30	PPD7	NEW	Printer Port Data Bit 7
31	/LED	NEW	LED (Audio filter bypass) Setting
32	GND	-	Digital Ground
33	RAWLF	NEW	Raw (Unfiltered) Audio Left
34	AGND	-	Audio Ground
35	RAWRT	NEW	Raw (Unfiltered) Audio Right
36	AGND	-	Audio Ground
37	n/c	-	Reserved for future expansion
38	n/c	-	Reserved for future expansion
39	GND	-	Digital Ground
40	GND	-	Digital Ground
41	n/c	-	Reserved for future expansion
42	n/c	-	Reserved for future expansion
43	GND	-	Digital Ground
44	GND	-	Digital Ground
45	RGB18	NEW	Red Bit 2
46	RGB19	NEW	Red Bit 3
47	RGB8	NEW	Green Bit 0
48	RGB9	NEW	Green Bit 1
49	RGB10	NEW	Green Bit 2
50	RGB11	NEW	Green Bit 3
51	RGB0	NEW	Blue Bit 0
52	RGB1	NEW	Blue Bit 1
53	RGB2	NEW	Blue Bit 2
54	RGB3	NEW	Blue Bit 3

Note: Direction is Motherboard relative Card.
Note: Do not mix analog & digital grounds.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

CD32 Expansion-port Connector

NEW
NEW
NEW

CD32 Expansion-port

NEW (At the computer)
UNKNOWN 182 PIN CONNECTOR (SAME AS MCA) at the computer.

Pin	Name	Description	Comment
1	A31	Address 31	Probably not connected since 68EC020
2	A30	Address 30	Probably not connected since 68EC020
3	A29	Address 29	Probably not connected since 68EC020
4	A28	Address 28	Probably not connected since 68EC020
5	A27	Address 27	Probably not connected since 68EC020
6	A26	Address 26	Probably not connected since 68EC020
7	A25	Address 25	Probably not connected since 68EC020
8	A24	Address 24	
9	DGND	Data Ground	
10	VCC	+5 VDC	
11	A23	Address 23	
12	A22	Address 22	
13	A21	Address 21	
14	A20	Address 20	
15	A19	Address 19	
16	A18	Address 18	
17	A17	Address 17	
18	A16	Address 16	
19	DGND	Data Ground	
20	VCC	+5 VDC	
21	A15	Address 15	
22	A14	Address 14	
23	A13	Address 13	
24	A12	Address 12	
25	A11	Address 11	
26	A10	Address 10	
27	A9	Address 9	
28	A8	Address 8	
29	DGND	Data Ground	
30	VCC	+5 VDC	
31	A7	Address 7	
32	A6	Address 6	
33	A5	Address 5	
34	A4	Address 4	
35	A3	Address 3	
36	A2	Address 2	
37	A1	Address 1	
38	A0	Address 0	
39	DGND	Data Ground	
40	VCC	+5 VDC	
41	D31	Data 31	
42	D30	Data 30	
43	D29	Data 29	
44	D28	Data 28	
45	D27	Data 27	

46	D26	Data 26	
47	D25	Data 25	
48	D24	Data 24	
49	DGND	Data Ground	
50	VCC	+5 VDC	
51	D23	Data 23	
52	D22	Data 22	
53	D21	Data 21	
54	D20	Data 20	
55	D19	Data 19	
56	D18	Data 18	
57	D17	Data 17	
58	D16	Data 16	
59	DGND	Data Ground	
60	VCC	+5 VDC	
61	D15	Data 15	
62	D14	Data 14	
63	D13	Data 13	
64	D12	Data 12	
65	D11	Data 11	
66	D10	Data 10	
67	D9	Data 9	
68	D8	Data 8	
69	DGND	Data Ground	
70	VCC	+5 VDC	
71	D7	Data 7	
72	D6	Data 6	
73	D5	Data 5	
74	D4	Data 4	
75	D3	Data 3	
76	D2	Data 2	
77	D1	Data 1	
78	D0	Data 0	
79	DGND	Data Ground	
80	VCC	+5 VDC	
81	/IPL2	Interrupt Priority Level 2	
82	/IPL1	Interrupt Priority Level 1	
83	/IPL0	Interrupt Priority Level 0	
84			
85	/RST	Reset	
86	/HALT	Halt	
87	/ECS	ECS??	
88	/OCS	OCS??	
89	SIZE1	Size 1	Indicates number of bytes remaining to transfer
90	SIZE0	Size 0	Indicates number of bytes remaining to transfer
91	/AS	Address Strobe	
92	/DS	Data Strobe	
93	/R/W	Read/Write	
94	/BERR	Bus Error	
95			
96	/AVEC	Autovector Req	Autovector request during interrupt acknowledge
97	/DSACK1	Data Ack 1	Data trasnfer and size acknowledge
98	/DSACK0	Data Ack 0	Data transfer and size acknowledge
99	CPUCLK_A		
100			
101	DGND	Data Ground	

102	VCC	+5 VDC	
103	FC2	Function Codes 2	
104	FC1	Function Codes 1	
105	FC0	Function Codes 0	
106			
107			
108			
109			
110			
111	/CPU_BR	CPU bus request??	
112	/EXP_BG	Expansion bus granted??	
113	/CPU_BG	CPU bus granted??	
114	/EXP_BR	Expansion bus request??	
115			
116			
117	/PUNT		
118	/RESET	68020 RESET	
119	/INT2	Interrupt 2	Generate a level 2 interrupt
120	/INT6	Interrupt 2	Generate a level 6 interrupt
121	/KB_CLOCK	Keyboard clock	
122	/KB_DATA	Keyboard data	
123	/FIRE0	Fire Button 0??	
124	/FIRE1	Fire Button 1??	
125	/LED	Power On LED ??	
126	/ACTIVE	Disk active LED	
127	/RXD	Serial Recieve	Serial data in
128	/TXD	Serial Transmit	Serial data out
129	/DKRD		Floppy interface (Paula?)
130	/DKWD		Floppy interface (Paula?)
131	SYSTEM		
132	/DKWE		Floppy interface (Paula?)
133	CONFIG_OUT		
134			
135	DGND	Data Ground	
136	+12V	+12V DC	
137	DGND	Data Ground	
138	+12V	+12V DC	
139	17MHZ		For FMV inteface ??
140	EXT_AUDIO		For FMV inteface ??
141	DA_DATA		For FMV inteface ??
142	/MUTE		For FMV inteface ??
143	DA_LRCLK		For FMV inteface ??
144	DA_BCLK		For FMV inteface ??
145	DGND	Data Ground	
146	VCC	+5 VDC	
147	DR	Digital Red	
148	DG	Digital Green	
149	DB	Digital Blue	
150	DI	Digital Intensity	
151	/PIXELSW_EXT		
152	/PIXELSW		
153	/BLANK		
154	PIXELCLK	Pixelclock	For manipulating RBG data
155	DGND	Data Ground	
156	VCC	+5 VDC	
157	/CSYNC	Composite sync	Not buffered.

158	CCK_B	Color clock ??	
159	/HSYNC	Horizontal sync	
160	/VSYNC	Vertical sync	
161	VGND	Video ground	
162	VGND	Video ground	
163	AR_EXT	Analog Red External	
164	AR	Analog Red	
165	AG_EXT	Analog Green External	
166	AG	Analog Green	
167	AB_EXT	Analog Blue External	
168	AB	Analog Blue	
169	VGND	Video ground	
170	VGND	Video ground	
171	/NTSC		
172	/XCLKEN	Enable External video clock	(Genlock)
173	XCLK	External video clock	(Genlock)
174	/EXT_VIDEO	External Video	Disable internal video interfaces
175	DGND	Data Ground	
176	VCC	+5 VDC	
177	AGND	Audio Ground	
178	+12V	+12V DC	
179	LEFT_EXT	Left sound External	
180	LEFT	Left sound	
181	RIGHT_EXT	Right sound External	
182	RIGHT	Right sound	

Contributor: Joakim Ogren

Source:CD32 expanstion port info, usenet posting by Anders Stenkvist..

Please send any comments to Joakim Ogren.

This is the URL for the ftp:
ftp://ftp.demon.co.uk/pub/amiga/docs/cd32-pinouts.txt
Open this address in your WWW browser or FTP client.

This the e-mail address:

ask_me@elixir.e.kth.se

Choose this address in your e-mail reader.

CardBus Connector

NEW
NEW
NEW

CardBus

32-bit bus defined by PCMCIA.

NEW (At the controller)

NEW (At the peripherals)

68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Name	Description
1	GND	Ground
2	CAD0	Address/Data 0
3	CAD1	Address/Data 1
4	CAD3	Address/Data 3
5	CAD5	Address/Data 5
6	CAD7	Address/Data 7
7	CCBE0#	Command/Byte Enable 0
8	CAD9	Address/Data 9
9	CAD11	Address/Data 11
10	CAD12	Address/Data 12
11	CAD14	Address/Data 14
12	CCBE1#	Command/Byte Enable 1
13	CPAR	Parity
14	CPERR#	Parity error
15	CGNT#	Grant
16	CINT#	Interrupt
17	Vcc	Vcc
18	Vpp1	Vpp1
19	CCLK	CCLK
20	CIRDY#	Initiator Ready
21	CCBE2#	Command/Byte Enable 2
22	CAD18	Address/Data 18
23	CAD20	Address/Data 20
24	CAD21	Address/Data 21
25	CAD22	Address/Data 22
26	CAD23	Address/Data 23
27	CAD24	Address/Data 24
28	CAD25	Address/Data 25
29	CAD26	Address/Data 26
30	CAD27	Address/Data 27
31	CAD29	Address/Data 29
32	RSRVD	Reserved
33	CCLKRUN#	CCLKRUN#
34	GND	Ground
35	GND	Ground
36	CCD1#	Card Detect 1
37	CAD2	Address/Data 2
38	CAD4	Address/Data 4
39	CAD6	Address/Data 6
40	RSRVD	Reserved

41	CAD8	Address/Data 8
42	CAD10	Address/Data 10
43	CVS1	
44	CAD13	Address/Data 13
45	CAD15	Address/Data 15
46	CAD16	Address/Data 16
47	RSRVD	Reserved
48	CBLOCK#	Block ???
49	CSTOP#	Stop transfer cycle
50	CDEVSEL#	Device Select
51	Vcc	Vcc
52	Vpp2	Vpp2
53	CTRDY#	Target Ready
54	CFRAME#	Address or Data phase
55	CAD17	Address/Data 17
56	CAD19	CAD19
57	CVS2	
58	CRST#	Reset
59	CSERR#	System Error
60	CREQ#	Request ???
61	CCBE3#	Command/Byte Enable 3
62	CAUDIO	Audio ???
63	CSTSCHG	
64	CAD28	Address/Data 28
65	CAD30	Address/Data 30
66	CAD31	Address/Data 31
67	CCD2#	Card Detect 2
68	GND	Ground

Contributor: Joakim Ogren

Source:PC Card Standard at PC Card's homepage

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.pc-card.com/stand_overview.html
Open this address in your WWW browser.

This is the URL for the WWW page:
http://www.pc-card.com
Open this address in your WWW browser.

PC Card Connector

NEW
NEW
NEW

PC Card

16-bit bus defined by PCMCIA.

NEW (At the controller)

NEW (At the peripherals)

68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Memory	I/O+Mem	Description
1	GND	GND	Ground
2	D3	D3	Data 3
3	D4	D4	Data 4
4	D5	D5	Data 5
5	D6	D6	Data 6
6	D7	D7	Data 7
7	CE1#	CE1#	
8	A10	A10	Address 10
9	OE#	OE#	Output Enable
10	A11	A11	Address 11
11	A9	A9	Address 9
12	A8	A8	Address 8
13	A13	A13	Address 13
14	A14	A14	Address 14
15	WE#	WE#	Write Enable ???
16	READY	IREQ#	
17	Vcc	Vcc	Vcc
18	Vpp1	Vpp1	Vpp1
19	A16	A16	Address 16
20	A15	A15	Address 15
21	A12	A12	Address 12
22	A7	A7	Address 7
23	A6	A6	Address 6
24	A5	A5	Address 5
25	A4	A4	Address 4
26	A3	A3	Address 3
27	A2	A2	Address 2
28	A1	A1	Address 1
29	A0	A0	Address 0
30	D0	D0	Data 0
31	D1	D1	Data 1
32	D2	D2	Data 2
33	WP	IOIS16#	
34	GND	GND	Ground
35	GND	GND	Ground
36	CD1#	CD1#	Card Detect 1
37	D11	D11	Data 11
38	D12	D12	Data 12
39	D13	D13	Data 13
40	D14	D14	Data 14

41	D15	D15	Data 15
42	CE2#	CE2#	
43	VS1#	VS1#	
44	RSRVD	IORD#	Reserved / IORD#
45	RSRVD	IOWR#	Reserved / IOWR#
46	A17	A17	Address 17
47	A18	A18	Address 18
48	A19	A19	Address 19
49	A20	A20	Address 20
50	A21	A21	Address 21
51	Vcc	Vcc	Vcc
52	Vpp2	Vpp2	Vpp2
53	A22	A22	Address 22
54	A23	A23	Address 23
55	A24	A24	Address 24
56	A25	A25	Address 25
57	VS2#	VS2#	
58	RESET	RESET	Reset
59	WAIT#	WAIT#	
60	RSRVD	INPACK#	Reserved / ???
61	REG#	REG#	
62	BVD2	SPKR#	Battery Voltage 2 / Speaker ???
63	BVD1	STSCHG#	Battery Voltage 1 / ???
64	D8	D8	Data 8
65	D9	D9	Data 9
66	D10	D10	Data 10
67	CD2#	CD2#	
68	GND	GND	Ground

Contributor: Joakim Ogren

Source:PC Card Standard at PC Card's homepage

Please send any comments to Joakim Ogren.

PC Card ATA Connector

NEW
NEW
NEW

PC Card ATA

This specification makes it possible to share ATA & PC Card with the same connectors.

NEW (At the controller)

NEW (At the peripherals)

68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Namel	Host	Dir	Dev	PC-Card equiv
1	Ground	x	NEW	x	Ground
2	DD3	x	NEW	x	D3
3	DD4	x	NEW	x	D4
4	DD5	x	NEW	x	D5
5	DD6	x	NEW	x	D6
6	DD7	x	NEW	x	D7
7	/CS0	x	NEW	x	/CE1
8			NEW	i	A10
9	/SELATA	x	NEW	x	/OE
10					
11	/CS1	x	NEW	x 1)	A9
12			NEW	i	A8
13					
14					
15			NEW	i	/WE
16	INTRQ	x	NEW	x	/READY:IREQ
17	VCC	x	NEW	x	VCC
18					
19					
20					
21					
22			NEW	i	A7
23			NEW	i	A6
24			NEW	i	A5
25			NEW	i	A4
26			NEW	i	A3
27	DA2	x	NEW	x	A2
28	DA1	x	NEW	x	A1
29	DA0	x	NEW	x	A0
30	DD0	x	NEW	x	D0
31	DD1	x	NEW	x	D1
32	DD2	x	NEW	x	D2
33	/IOCS16	x	NEW	x	/WP:IOIS16
34	Ground	x	NEW	x	Ground
35	Ground	x	NEW	x	Ground
36	/CD1	x	NEW	x	/CD1
37	DD11	x	NEW	x	D11
38	DD12	x	NEW	x	D12
39	DD13	x	NEW	x	D13
40	DD14	x	NEW	x	D14

41	DD15	x	NEW	x	D15
42	/CS1	x	NEW	x 1)	/CE2
43			NEW	i	/VS1
44	/DIOR	x	NEW	x	/IORD
45	/DIOW	x	NEW	x	/IOWR
46					
47					
48					
49					
50					
51	VCC	x	NEW	x	VCC
52					
53					
54					
55	M/S-	x	NEW	x 2)	
56	CSEL	x	NEW	x 2)	
57			NEW	i	/VS2
58	/RESET	x	NEW	x	RESET
59	IORDY	o	NEW	x 3)	/WAIT
60	DMARQ	o	NEW	x 3)	/INPACK
61	/DMACK	o	NEW	o	/REG
62	/DASP	x	NEW	x	/BVD2:SPKR
63	/PDIAG	x	NEW	x	/BVD1:STSCHG
64	DD8	x	NEW	x	D8
65	DD9	x	NEW	x	D9
66	DD10	x	NEW	x	D10
67	/CD2	x	NEW	x	/CD2
68	Ground	x	NEW	x	Ground

x = Required.
i = Ignored by host in ATA mode.
o = Optional.
nothing = Not connected.
1) Device shall support only one /CS1 signal pin.
2) Device shall support either /M/S or CSEL but not both.
3) Device shall hold this signal negated if it does not support this function.

Contributor: Joakim Ogren

Source:ATA-2 specifictions

Please send any comments to Joakim Ogren.

PCMCIA Connector

NEW
NEW
NEW

PCMCIA

PCMCIA=Personal Computer Memory Card International Association.

NEW (At the controller)

NEW (At the peripherals)

68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Name	Description
1	GND	Ground
2	D3	Data 3
3	D4	Data 4
4	D5	Data 5
5	D6	Data 6
6	D7	Data 7
7	/CE1	Card Enable 1
8	A10	Address 10
9	/OE	Output Enable
10	A11	Address 11
11	A9	Address 9
12	A8	Address 8
13	A13	Address 13
14	A14	Address 14
15	/WE:/P	Write Enable : Program
16	/READY:/IREQ	Ready : Busy (IREQ)
17	VCC	+5V
18		Vpp1
19	A16	Address 16
20	A15	Address 15
21	A12	Address 12
22	A7	Address 7
23	A6	Address 6
24	A5	Address 5
25	A4	Address 4
26	A3	Address 3
27	A2	Address 2
28	A1	Address 1
29	A0	Address 0
30	D0	Data 0
31	D1	Data 1
32	D2	Data 2
33	/WP:/IOIS16	Write Protect : IOIS16
34	GND	Ground
35	GND	Ground
36	/CD1	Card Detect 1
37	D11	Data 11
38	D12	Data 12
39	D13	Data 13
40	D14	Data 14

41	D15	Data 15
42	/CE2	Card Enable 2
43	/VS1	Refresh
44	/IORD	I/O Read
45	/IOWR	I/O Write
46	A17	Address 17
47	A18	Address 18
48	A19	Address 19
49	A20	Address 20
50	A21	Address 21
51	VCC	+5V
52		Vpp2
53	A22	Address 22
54	A23	Address 23
55	A24	Address 24
56	A25	Address 25
57	/VS2	RFU
58	RESET	RESET
59	/WAIT	WAIT
60	/INPACK	
61	/REG	Register Select
62	/BVD2:SPKR	Battery Voltage Detect 2 : SPKR
63	/BVD1:STSCHG	Battery Voltage Detect 1 : STSCHG
64	D8	Data 8
65	D9	Data 9
66	D10	Data 10
67	/CD2	Card Detect 2
68	GND	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

CompactFlash Connector

NEW
NEW
NEW

CompactFlash

Developed by SanDisk.
Is compatible with PC-Card ATA with a simple passive adapter.

See PC-Card ATA for more information.

NEW (At the controller)

NEW (At the peripherals)
50 PIN ??? MALE at the controller.
50 PIN ??? FEMALE at the peripherals.

Pin	Name	Description
1	GND	Ground
2	D3	Data 3
3	D4	Data 4
4	D5	Data 5
5	D6	Data 6
6	D7	Data 7
7	/CE1	Card Enable 1
8	A10	Address 10
9	/OE	Output Enable
10	A9	Address 9
11	A8	Address 8
12	A7	Address 7
13	VCC	+5V
14	A6	Address 6
15	A5	Address 5
16	A4	Address 4
17	A3	Address 3
18	A2	Address 2
19	A1	Address 1
20	A0	Address 0
21	D0	Data 0
22	D1	Data 1
23	D2	Data 2
24	/WP:/IOIS16	Write Protect : IOIS16
25	/CD2	Card Detect 2
26	/CD1	Card Detect 1
27	D0	Data 0
28	D0	Data 0
29	D0	Data 0
30	D0	Data 0
31	D0	Data 0
32	/CE2	Card Enable 2
33	/VS1	Refresh
34	/IORD	I/O Read
35	/IOWR	I/O Write
36	/WE	Write Enable
37	/READY:/RDY:/IREQ	Ready : Busy : IREQ

38	VCC	+5V
39	CSEL	
40	/VS2	RFU
41	RESET	Reset
42	/WAIT	Wait
43	/INPACK	
44	/REG	Register Select
45	/BVD2:SPKR	Battery Voltage Detect 2 : SPKR
46	/BVD1:STSCHG	Battery Voltage Detect 1 : STSCHG
47	D8	Data 8
48	D9	Data 9
49	D10	Data 10
50	GND	Ground

Contributor: Joakim Ogren

Source:SanDisk's CompactFlash ABC at SanDisk's homepage

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.sandisk.com/sd/support/teched/cfpc_5.htm
Open this address in your WWW browser.

This is the URL for the WWW page:
http://www.sandisk.com
Open this address in your WWW browser.

C-bus II Connector

NEW
NEW
NEW

C-bus II

Developed by Corolla
C-bus II is the successor to C-bus & Extended C-bus.

NEW (At the backplane)

NEW (At the device (card))

UNKNOWN CONNECTOR at the backplane.
UNKNOWN CONNECTOR at the device (card).
PA=Component side
PB=Solder side

Pin	Name
PA1	GND
PA2	AUX18
PA3	AUX16
PA4	GND
PA5	AUX14
PA6	AUX12
PA7	GND
PA8	AUX10
PA9	AUX8
PA10	GND
PA11	AUX6
PA12	AUX4
PA13	GND
PA14	AUX2
PA15	AUX0
PA16	GND
PA17	RESERVED8
PA18	RESERVED6
PA19	RESERVED4
PA20	RESERVED2
PA21	RESERVED0
PA22	GND
PA23	GND
PA24	AGND
PA25	CID1
PA26	CBCLK
PA27	GND
PA28	CRST#
PA29	LED#
PA30	GND
PA31	CARB2
PA32	CARB0
PA33	GND
PA34	TM2#
PA35	TM0#
PA36	GND

PA37	STRT#
PA38	CD31
PA39	GND
PA40	CD30
PA41	CD29
PA42	GND
PA43	CD28
PA44	CD27
PA45	GND
PA46	CD26
PA47	CD25
PA48	GND
PA49	CD24
PA50	CD23
PA51	GND
PA52	CD22
PA53	CD21
PA54	GND
PA55	CD20
PA56	CD19
PA57	GND
PA58	CD18
PA59	CD17
PA60	GND
PA61	CD16
PA62	E3
PA63	GND
PA64	E2
PA65	CD15
PA66	GND
PA67	CD14
PA68	CD13
PA69	GND
PA70	CD12
PA71	CD11
PA72	GND
PA73	CD10
PA74	CD9
PA75	GND
PA76	CD8
PA77	CD7
PA78	GND
PA79	CD6
PA80	CD5
PA81	GND
PA82	CD4
PA83	CD3
PA84	GND
PA85	CD2
PA86	CD1
PA87	GND
PA88	CD0
PA89	E1
PA90	GND
PA91	E0

PB1	+5V
PB2	AUX19
PB3	AUX17
PB4	+5V
PB5	AUX15
PB6	AUX13
PB7	+5V
PB8	AUX11
PB9	AUX9
PB10	+5V
PB11	AUX7
PB12	AUX5
PB13	+5V
PB14	AUX3
PB15	AUX1
PB16	+5V
PB17	RESERVED9
PB18	RESERVED7
PB19	RESERVED5
PB20	RESERVED3
PB21	RESERVED1
PB22	VTERM
PB23	+5V
PB24	CID3
PB25	CID2
PB26	CID0
PB27	+5V
PB28	FAULT#
PB29	LOCKCB#
PB30	+5V
PB31	CARB3
PB32	CARB1
PB33	+5V
PB34	TM3#
PB35	TM1#
PB36	+5V
PB37	ACK#
PB38	CD63
PB39	+5V
PB40	CD62
PB41	CD61
PB42	+5V
PB43	CD60
PB44	CD59
PB45	+5V
PB46	CD58
PB47	CD57
PB48	+5V
PB49	CD56
PB50	CD55
PB51	+3.3V
PB52	CD54
PB53	CD53
PB54	+3.3V
PB55	CD52
PB56	CD51

PB57	+3.3V
PB58	CD50
PB59	CD49
PB60	+3.3V
PB61	CD48
PB62	E7
PB63	+3.3V
PB64	E6
PB65	CD47
PB66	+3.3V
PB67	CD46
PB68	CD45
PB69	+3.3V
PB70	CD44
PB71	CD43
PB72	+3.3V
PB73	CD42
PB74	CD41
PB75	+3.3V
PB76	CD40
PB77	CD39
PB78	+3.3V
PB79	CD38
PB80	CD37
PB81	+3.3V
PB82	CD36
PB83	CD35
PB84	+3.3V
PB85	CD34
PB86	CD33
PB87	+3.3V
PB88	CD32
PB89	E5
PB90	+3.3V
PB91	E4

Contributor: Joakim Ogren

Sources:C-bus II Technology architecture at Collary's homepage

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.corollary.com/cbusii.html
Open this address in your WWW browser.

This is the URL for the WWW page:
http://www.collary.com
Open this address in your WWW browser.

SSFDC Connector

NEW
NEW
NEW

SSFDC

SSFDC=Solid State Floppy Disk Card.

NEW (At the motherboard)

NEW (At the device)

UNKNOWN CONNECTOR at the motherboard.

UNKNOWN CONNECTOR at the device.

I don't have any technical information about SSFDC at the moment. If you have any information of value please send it to me.

Contributor: Joakim Ogren

Source:?

Info: Solid State Floppy Disk Card Forum

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.ssfdc.com
Open this address in your WWW browser.

PC/104 Connector

NEW
NEW
NEW

PC/104

NEW (At the backplane)

NEW (At the device (card))

UNKNOWN CONNECTOR at the backplane.

UNKNOWN CONNECTOR at the device (card).

Pin Number	J1/P1 Row A	J1/P1 Row B	J2/P2 Row C1	J2/P2 Row D1
0	--	--	0V	0V
1	IOCHCHK*	0V	SBHE*	MEMCS16*
2	SD7	RESETDRV	LA23	IOCS16*
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	ENDXFR*	LA17	DACK0*
9	SD0	+12V	MEMR*	DRQ0
10	IOCHRDY	(KEY)2	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*
15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	DACK1*	SD14	MASTER*
18	SA13	DRQ1	SD15	0V
19	SA12	REFRESH*		(KEY)2 0V
20	SA11	SYSCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	IRQ6	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4	--	--
25	SA6	IRQ3	--	--
26	SA5	DACK2*	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5V	--	--
30	SA1	OSC	--	--
31	SA0	0V	--	--
32	0V	0V	--	--

Contributor: Joakim Ogren

Sources:PC/104 v2.3 spec

Sources:PC/104 pinout

Info:PC/104 Consortium

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.pc104.org/pc104/consp5.html
Open this address in your WWW browser.

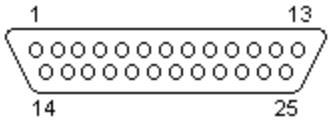
This is the URL for the WWW page:
http://www.pc104.org/pc104/pinouts.html
Open this address in your WWW browser.

This is the URL for the WWW page:
http://www.pc104.org/pc104/consp1.html
Open this address in your WWW browser.

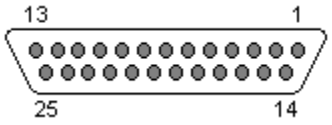
RS232 Connector

NEW
NEW
NEW

RS232



(At the DTE)



(At the DCE)

25 PIN D-SUB MALE at the DTE (Computer).
25 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Name	ITU-T	Dir	Description
1	GND	101	-	Shield Ground
2	TXD	103	NEW	Transmit Data
3	RXD	104	NEW	Recieve Data
4	RTS	105	NEW	Request to Send
5	CTS	106	NEW	Clear to Send
6	DSR	107	NEW	Data Set Ready
7	GND	102	-	System Ground
8	CD	109	NEW	Carrier Detect
9	-		-	RESERVED
10	-		-	RESERVED
11	STF	126	NEW	Select Transmit Channel
12	S.CD	?	NEW	Secondary Carrier Detect
13	S.CTS	?	NEW	Secondary Clear to Send
14	S.TXD	?	NEW	Secondary Transmit Data
15	TCK	114	NEW	Transmission Signal Element Timing
16	S.RXD	?	NEW	Secondary Recieve Data
17	RCK	115	NEW	Reciever Signal Element Timing
18	LL	141	NEW	Local Loop Control
19	S.RTS	?	NEW	Secondary Request to Send
20	DTR	108	NEW	Data Terminal Ready
21	RL	140	NEW	Remote Loop Control
22	RI	125	NEW	Ring Indicator
23	DSR	111	NEW	Data Signal Rate Selector
24	XCK	113	NEW	Transmit Signal Element Timing
25	TI	142	NEW	Test Indicator

Note: Direction is DTE (Computer) relative DCE (Modem).
Note: Do not connect SHIELD(1) to GND(7).

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Serial (PC 9) Connector

NEW
NEW
NEW

Serial (PC 9)

NEW (At the Computer)

9 PIN D-SUB MALE at the Computer.

Pin	Name	Dir	Description
1	CD	NEW	Carrier Detect
2	RXD	NEW	Recieve Data
3	TXD	NEW	Transmit Data
4	DTR	NEW	Data Terminal Ready
5	GND	-	System Ground
6	DSR	NEW	Data Set Ready
7	RTS	NEW	Request to Send
8	CTS	NEW	Clear to Send
9	RI	NEW	Ring Indicator

Note: Direction is DTE (Computer) relative DCE (Modem).

Contributor: Joakim Ogren

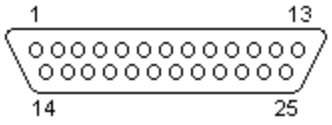
Source:?

Please send any comments to Joakim Ogren.

Serial (PC 25) Connector

NEW
NEW
NEW

Serial (PC 25)



(At the computer)

25 PIN D-SUB MALE at the computer.

Pin	Name	Dir	Description
1	SHIELD	-	Shield Ground
2	TXD	NEW	Transmit Data
3	RXD	NEW	Recieve Data
4	RTS	NEW	Request to Send
5	CTS	NEW	Clear to Send
6	DSR	NEW	Data Set Ready
7	GND	-	System Ground
8	CD	NEW	Carrier Detect
9	n/c	-	
10	n/c	-	
11	n/c	-	
12	n/c	-	
13	n/c	-	
14	n/c	-	
15	n/c	-	
16	n/c	-	
17	n/c	-	
18	n/c	-	
19	n/c	-	
20	DTR	NEW	Data Terminal Ready
21	n/c	-	
22	RI	NEW	Ring Indicator
23	n/c	-	
24	n/c	-	
25	n/c	-	

Note: Direction is DTE (Computer) relative DCE (Modem).
Note: Do not connect SHIELD(1) to GND(7).

Contributor: Joakim Ogren

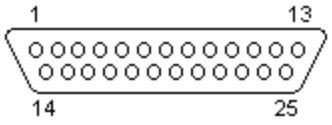
Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

Serial (Amiga 1000) Connector

NEW
NEW
NEW

Serial (Amiga 1000)



(At the Amiga 1000)

25 PIN D-SUB MALE at the Amiga 1000.

Pin	Name	Dir	Description
1	SHIELD	―	Shield Ground
2	TXD	NEW	Transmit Data
3	RXD	NEW	Recieve Data
4	RTS	NEW	Request to Send
5	CTS	NEW	Clear to Send
6	DSR	NEW	Data Set Ready
7	GND	―	System Ground
8	CD	NEW	Carrier Detect
9	n/c	-	
10	n/c	-	
11	n/c	-	
12	n/c	-	
13	n/c	-	
14	-5V	NEW	-5 Volts DC (50mA max)
15	AUDO	NEW	Amiga Audio Out (Left)
16	AUDI	NEW	Amiga Audio In (Right)
17	EB	-	EB=Buffered Port Clock 716 kHz
18	/INT2	?	Interrupt 2
19	n/c	-	
20	DTR	NEW	Data Terminal Ready
21	+5V	NEW	+5 Volts DC
22	n/c	-	
23	+12V	NEW	+12 Volts DC (20 mA max)
24	/C2	NEW	C2=Clock 3.58MHz
25	/RESET	NEW	Reset

Note: Direction is DTE (Computer) relative DCE (Modem).
Note: Do not connect SHIELD(1) to GND(7).

Contributor: Joakim Ogren

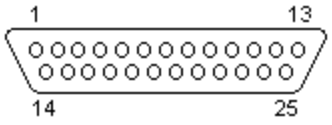
Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

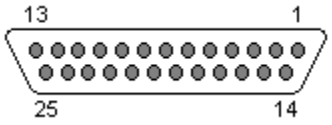
Serial (Amiga) Connector

NEW
NEW
NEW

Serial (Amiga)



(At the computer)



(At the cable)

25 PIN D-SUB MALE at the computer.
25 PIN D-SUB FEMALE at the cable.

Pin	Name	Dir	Description
1	SHIELD	—	Shield Ground
2	TXD	NEW	Transmit Data
3	RXD	NEW	Recieve Data
4	RTS	NEW	Request to Send
5	CTS	NEW	Clear to Send
6	DSR	NEW	Data Set Ready
7	GND	—	System Ground
8	CD	NEW	Carrier Detect
9	+12V	NEW	+12 Volts DC (20 mA max)
10	-12V	NEW	-12 Volts DC (20 mA max)
11	AUDO	NEW	Amiga Audio Out (Left)
12	n/c	-	Speed Indicate
13	n/c	-	
14	n/c	-	
15	n/c	-	
16	n/c	-	
17	n/c	-	
18	AUDI	NEW	Amiga Audio In (Right)
19	n/c	-	
20	DTR	NEW	Data Terminal Ready
21	n/c	-	
22	RI	NEW	Ring Indicator
23	n/c	-	
24	n/c	-	
25	n/c	-	

Note: Direction is DTE (Computer) relative DCE (Modem).
Note: Do not connect SHIELD(1) to GND(7).

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

Serial (MSX) Connector

NEW
NEW
NEW

Serial (MSX)

NEW (At the Computer)

9 PIN D-SUB FEMALE at the Computer.

Pin	Name	Dir	Description
1	PG	-	Protective Ground
2	TXD	NEW	Transmit Data
3	RXD	NEW	Recieve Data
4	RTS	NEW	Request to Send
5	CTS	NEW	Clear to Send
6	DSR	NEW	Data Set Ready
7	GND	-	Signal Ground
8	DCD	NEW	Carrier Detect
9	DTR	NEW	Data Terminal Ready

Note: Direction is DTE (Computer) relative DCE (Modem).

Contributor: Joakim Ogren

Source:Mayer's SV738 X'press I/O map

Please send any comments to Joakim Ogren.

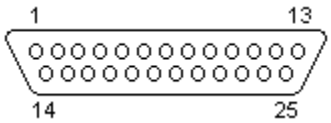
This is the URL for the WWW page:
http://www.freeflight.com/fms/MSX/Portar.txt
Open this address in your WWW browser.

DEC Dual RS-232 Connector

NEW
NEW
NEW

DEC Dual RS-232

Found on the DEC Multia and DEC UDB. It contains two Serial ports on one connector. The 1st Port is located on the normal pins, and the 2nd port is located on some "spare" pins.



(At the computer)

25 PIN D-SUB MALE at the computer.

Pin	Port	Name	Dir	Description
1		n/c		Not connected
2	1	TXD	NEW	Transmit Data
3	1	RXD	NEW	Receive Data
4	1	RTS	NEW	Ready To Send
5	1	CTS	NEW	Clear To Send
6	1	DSR	NEW	Data Set Ready
7	1+2	GND	-	Ground
8	1	DCD	NEW	Data Carrier Detect
9		n/c		Not connected
10		n/c		Not connected
11	2	DTR	NEW	Data Terminal Ready
12	2	DCD	NEW	Data Carrier Detect
13	2	CTS	NEW	Clear To Send
14	2	TXD	NEW	Transmit Data
15		n/c		Not connected
16	2	RXD	NEW	Recieve Data
17		n/c		Not connected
18		n/c		Not connected
19	2	RTS	NEW	Ready To Send
20	1	DTR	NEW	Data Terminal Ready
21		n/c		Not connected
22	1	RI	NEW	Ring Indicator
23	2	DSR	NEW	Data Set Ready
24		n/c		Not connected
25	2	RI	NEW	Ring Indicator

Note: Direction is DTE (Computer) relative DCE (Modem).

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://csgrad.cs.vt.edu/~tjohnson/pinouts
Open this address in your WWW browser.

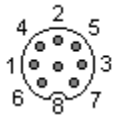
This the e-mail address:
tjohnson@csgrad.cs.vt.edu
Choose this address in your e-mail reader.

Macintosh RS-422 Connector

NEW
NEW
NEW

Macintosh RS-422

It's possible to connect RS-232 peipheral to the RS-422 port availble on Macintosh computers. Use RXD- as RXD, TXD- as TXD, Ground RXD+, Leave TXD+ unconnected, GPi as CD.



(At the computer)

8 PIN DIN (DIN45326) FEMALE at the computer.

Pin	Name	Dir	Description
1	HSKo	NEW	Output Handshake
2	HSKi/CLK	NEW	Input Handshake or External Clock
3	TXD-	NEW	Transmit Data (-)
4	GND	-	Ground
5	RXD-	NEW	Receive Data (-)
6	TXD+	NEW	Transmit Data (+)
7	n/c	-	No connection
8	RXD+	NEW	Receive Data (+)

Note: Direction is DTE (Computer) relative DCE (Modem).

Contributor: Joakim Ogren

Source: comp.sys.mac.comm FAQ Part 1

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.cis.ohio-state.edu/hypertext/faq/usenet/macintosh/comm-faq/part1/faq.html
Open this address in your WWW browser.

C64 RS232 User Port Connector

NEW
NEW
NEW

C64 RS232 User Port

Availble on the Commodore C64/C128. Software emulated. The signals does not have true RS232 levels. It's TTL level, and RXD/TXD is inverted.

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	RS232	Description
A	GND	GND	Protective Ground
B+C	FLAG2+PB0	RxD	Recieve Data (Must be applied to both pins!)
D	PB1	RTS	Ready To Send
E	PB2	DTR	Data Terminal Ready
F	PB3	RI	Ring Indicator
H	PB4	DCD	Data Carrier Detect
K	PB6	CTS	Clear To Send
L	PB7	DSR	?
M	PA2	TxD	Transmit Data
N	GND	GND	Signal Ground

Contributor: Joakim Ogren

Source: Usenet posting in comp.sys.cbm, Help on modem - c64 by Lasher Glenn

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.vuse.vanderbilt.edu/~thompsbb/cbm_conn.txt
Open this address in your WWW browser.

This the e-mail address:
gl8574@lima.albany.edu
Choose this address in your e-mail reader.

Parallel (PC) Connector

NEW
NEW
NEW

Parallel (PC)

NEW (At the PC)
25 PIN D-SUB FEMALE at the PC.

Pin	Name	Dir	Description
1	/STROBE	NEW	Strobe
2	D0	NEW	Data Bit 0
3	D1	NEW	Data Bit 1
4	D2	NEW	Data Bit 2
5	D3	NEW	Data Bit 3
6	D4	NEW	Data Bit 4
7	D5	NEW	Data Bit 5
8	D6	NEW	Data Bit 6
9	D7	NEW	Data Bit 7
10	/ACK	NEW	Acknowledge
11	BUSY	NEW	Busy
12	PE	NEW	Paper End
13	SELIN	NEW	Select In
14	/AUTOFD	NEW	Autofeed
15	/ERROR	NEW	Error
16	/INIT	NEW	Initialize
17	/SEL	NEW	Select
18	GND	-	Signal Ground
19	GND	-	Signal Ground
20	GND	-	Signal Ground
21	GND	-	Signal Ground
22	GND	-	Signal Ground
23	GND	-	Signal Ground
24	GND	-	Signal Ground
25	GND	-	Signal Ground

Note: Direction is Computer relative Device.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Parallel (Amiga) Connector

NEW
NEW
NEW

Parallel (Amiga)

NEW (At the Amiga)

25 PIN D-SUB FEMALE at the Amiga.

Pin	Name	Dir	Description
1	/STROBE	NEW	Strobe
2	D0	NEW	Data Bit 0
3	D1	NEW	Data Bit 1
4	D2	NEW	Data Bit 2
5	D3	NEW	Data Bit 3
6	D4	NEW	Data Bit 4
7	D5	NEW	Data Bit 5
8	D6	NEW	Data Bit 6
9	D7	NEW	Data Bit 7
10	/ACK	NEW	Acknowledge
11	BUSY	NEW	Busy
12	POUT	NEW	Paper Out
13	SEL	NEW	Select (Shared with RS232 RING-indicator)
14	+5V PULLUP	-	+5 Volts DC (10 mA max)
15	n/c	-	Not connected.
16	/RESET	NEW	Reset
17	GND	-	Signal Ground
18	GND	-	Signal Ground
19	GND	-	Signal Ground
20	GND	-	Signal Ground
21	GND	-	Signal Ground
22	GND	-	Signal Ground
23	GND	-	Signal Ground
24	GND	-	Signal Ground
25	GND	-	Signal Ground

Note: Direction is Computer relative Peripheral.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

Parallel (Amiga 1000) Connector

NEW
NEW
NEW

Parallel (Amiga 1000)

NEW (At the Amiga 1000)
25 PIN D-SUB MALE at the Amiga 1000.

Pin	Name	Dir	Description
1	/STROBE	NEW	Strobe
2	D0	NEW	Data Bit 0
3	D1	NEW	Data Bit 1
4	D2	NEW	Data Bit 2
5	D3	NEW	Data Bit 3
6	D4	NEW	Data Bit 4
7	D5	NEW	Data Bit 5
8	D6	NEW	Data Bit 6
9	D7	NEW	Data Bit 7
10	/ACK	NEW	Acknowledge
11	BUSY	NEW	Busy
12	POUT	NEW	Paper Out
13	SEL	NEW	Select (Shared with RS232 RING-indicator)
14	GND	-	Signal Ground
15	GND	-	Signal Ground
16	GND	-	Signal Ground
17	GND	-	Signal Ground
18	GND	-	Signal Ground
19	GND	-	Signal Ground
20	GND	-	Signal Ground
21	GND	-	Signal Ground
22	GND	-	Signal Ground
23	+5V	-	+5 Volts DC (10 mA max)
24	n/c	-	Not connected.
25	/RESET	NEW	Reset

Note: Direction is Computer relative Peripheral.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

ECP Parallel Connector

NEW
NEW
NEW

ECP Parallel

ECP = Extended Capabilities Port

NEW (At the PC)

25 PIN D-SUB FEMALE at the PC.

Pin	Name	Dir	Description
1	nStrobe	NEW	Strobe
2	data0	NEW	Address, Data or RLE Data Bit 0
3	data1	NEW	Address, Data or RLE Data Bit 1
4	data2	NEW	Address, Data or RLE Data Bit 2
5	data3	NEW	Address, Data or RLE Data Bit 3
6	data4	NEW	Address, Data or RLE Data Bit 4
7	data5	NEW	Address, Data or RLE Data Bit 5
8	data6	NEW	Address, Data or RLE Data Bit 6
9	data7	NEW	Address, Data or RLE Data Bit 7
10	/nAck	NEW	Acknowledge
11	Busy	NEW	Busy
12	PError	NEW	Paper End
13	Select	NEW	Select In
14	/nAutoFd	NEW	Autofeed
15	/nFault	NEW	Error
16	/nInit	NEW	Initialize
17	/nSelectIn	NEW	Select
18	GND	-	Signal Ground
19	GND	-	Signal Ground
20	GND	-	Signal Ground
21	GND	-	Signal Ground
22	GND	-	Signal Ground
23	GND	-	Signal Ground
24	GND	-	Signal Ground
25	GND	-	Signal Ground

Note: Direction is Computer relative Device.

Contributor: Joakim Ogren

Source:Microsoft MSDN Library: Extended Capabilities Port Specs

Info: Microsoft MSDN Library

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.microsoft.com/msdn
Open this address in your WWW browser.

ECP Parallel (Technical)

This file is designed to give a basic overview of the port found in most newer PC computers called ECP Parallel port.

This file is not intended to be a thorough coverage of the standard. It is for informational purposes only, and is intended to give designers and hobbyists sufficient information to design their own ECP compatible devices.

Signal Descriptions:

nStrobe

This signal is registers data or address into the slave on the assering edge during .

data 0-7

Contains address, data or RLE data. Can be used in both directions.

nAck

Valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.

Busy

This signal deasserts to indicate that the peiheral can accept data. In forward direction this handshakes with nStrobe. In the reverse direction this signal indicates that the data is RLE compressed by being low.

PError

Used to acknowledge a change in the direction of transfer. High=Forward.

Select

Printer is online.

nAutoFd

Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data.

nFault

Generates an error interrupt when asserted.

nInit

Sets the transfer direction. High=Reverse, Low=Forward.

nSelectIn

Low in ECP mode.

Contributor: Joakim Ogren

Source:Microsoft MSDN Library: Extended Capabilities Port Specs

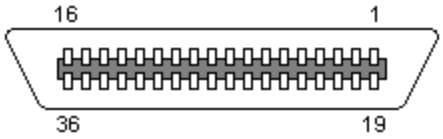
Info: Microsoft MSDN Library

Please send any comments to Joakim Ogren.

Centronics Connector

NEW
NEW
NEW

Centronics



(At the Printer)

36 PIN CENTRONICS FEMALE at the Printer.

Pin	Name	Dir	Description
1	/STROBE	NEW	Strobe
2	D0	NEW	Data Bit 0
3	D1	NEW	Data Bit 1
4	D2	NEW	Data Bit 2
5	D3	NEW	Data Bit 3
6	D4	NEW	Data Bit 4
7	D5	NEW	Data Bit 5
8	D6	NEW	Data Bit 6
9	D7	NEW	Data Bit 7
10	/ACK	NEW	Acknowledge
11	BUSY	NEW	Busy
12	POUT	NEW	Paper Out
13	SEL	NEW	Select
14	/AUTOFEED	?	Autofeed
15	n/c		
16	0 V		
17	CHASSIS GND		
18	+5 V PULLUP	-	+5 V DC (50 mA max)
19	GND	-	Signal Ground
20	GND	-	Signal Ground
21	GND	-	Signal Ground
22	GND	-	Signal Ground
23	GND	-	Signal Ground
24	GND	-	Signal Ground
25	GND	-	Signal Ground
26	GND	-	Signal Ground
27	GND	-	Signal Ground
28	GND	-	Signal Ground
29	GND	-	Signal Ground
30	/GNDRESET	-	Reset Ground
31	/RESET	NEW	Reset
32	/FAULT	NEW	Fault (Low when offline)
33	0 V	-	Signal Ground
34	n/c		
35	+5 V	NEW	+5 V DC
36	/SLCT IN	NEW	Select In (Taking low or high sets printer on line or off line respectively)

Note: Direction is Printer relative Computer.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

MSX Parallel Connector

NEW
NEW
NEW

MSX Parallel

NEW (At the Computer)

14 PIN CENTRONICS FEMALE at the Computer.

Pin	Name	Dir	Description
1	/STB	NEW	Strobe
2	PDB0	NEW	Data 0
3	PDB1	NEW	Data 1
4	PDB2	NEW	Data 2
5	PDB3	NEW	Data 3
6	PDB4	NEW	Data 4
7	PDB5	NEW	Data 5
8	PDB6	NEW	Data 6
9	PDB7	NEW	Data 7
10	n/c	-	
11	BUSY	NEW	Printer is busy
12	n/c	-	
13	n/c	-	
14	GND	-	Signal Ground

Note: Direction is Computer relative Printer.

Contributor: Joakim Ogren

Source:Mayer's SV738 X'press I/O map

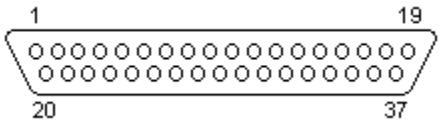
Please send any comments to Joakim Ogren.

GeekPort Connector

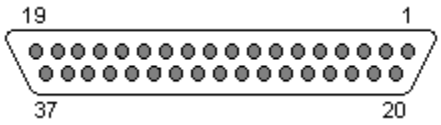
NEW
NEW
NEW

GeekPort

The GeekPort is a connector availble at Be's BeBox computers.
This is a dream for all hobby engineers who like to connect the computer to the coffee machine.



(At the device)



(At the computer)

37 PIN D-SUB MALE CONNECTOR at the device.
37 PIN D-SUB FEMALE CONNECTOR at the computer.

Pin	Name	Description	Dir
1	GND	Ground	
2	A1	Digital A 1	NEW
3	A3	Digital A 3	NEW
4	A5	Digital A 5	NEW
5	A7	Digital A 7	NEW
6	GND	Ground	
7	+5V	+5 VDC	
8	GND	Ground	
9	+12V	+12 VDC	
10	GND	Ground	
11	-12V	-12 VDC	
12	GND	Ground	
13	+5V	+5 VDC	
14	GND	Ground	
15	B0	Digital B 0	NEW
16	B2	Digital B 2	NEW
17	B4	Digital B 4	NEW
18	B6	Digital B 6	NEW
19	GND	Ground	
20	A0	Digital A 0	NEW
21	A2	Digital A 2	NEW
22	A4	Digital A 4	NEW
23	A6	Digital A 6	NEW
24	AIref	Analog In Reference	NEW
25	A2D1	Analog In 1	NEW
26	A2D2	Analog In 2	NEW
27	A2D3	Analog In 3	NEW
28	A2D4	Analog In 4	NEW
29	D2A1	Analog Out 1	NEW
30	D2A2	Analog Out 2	NEW
31	D2A3	Analog Out 3	NEW

32	D2A4	Analog Out 4	NEW
33	AOref	Analog Out Reference	NEW
34	B1	Digital B 1	NEW
35	B3	Digital B 3	NEW
36	B5	Digital B 5	NEW
37	B7	Digital B 7	NEW

Note: Direction is Computer relative Device.

Contributor: Joakim Ogren

Sources:BeBox GeekPort DeviceKit at Be's homepage
Sources:BeBox GeekPort DeviceKit: Analog port
Sources:BeBox GeekPort DeviceKit: Digital port

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.be.com/documentation/be_book/DeviceKit/geek.html
Open this address in your WWW browser.

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http://www.be.com
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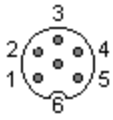
http://www.be.com/documentation/be_book/DeviceKit/A2D2A.html
Open this address in your WWW browser.

This is the URL for the WWW page:
http://www.be.com/documentation/be_book/DeviceKit/DPort.html
Open this address in your WWW browser.

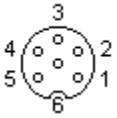
C64 Serial I/O Connector

NEW
NEW
NEW

C64 Serial I/O



(At the computer)



(At the cable)

6 PIN DIN (DIN45322) FEMALE at the Computer.
6 PIN DIN (DIN45322) MALE at the Cable.

Pin	Name	Description
1	/SRQIN	Serial SRQIN
2	GND	Ground
3	ATN	Serial ATN In/Out
4	CLK	Serial CLK In/Out
5	DATA	Serial DATA In/Out
6	/RESET	Reset

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

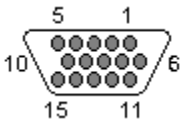
VGA (VESA DDC) Connector

NEW
NEW
NEW

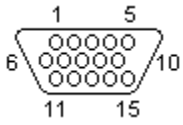
VGA (VESA DDC)

VGA=Video Graphics Adapter or Video Graphics Array.
VESA=Video Electronics Standards Association.
DDC=Display Data Channel.

Videotype: Analogue.



(At the videocard)



(At the monitor cable)

15 PIN HIGHDENSITY D-SUB FEMALE at the videocard.
15 PIN HIGHDENSITY D-SUB MALE at the monitor cable.

Pin	Name	Dir	Description
1	RED	NEW	Red Video (75 ohm, 0.7 V p-p)
2	GREEN	NEW	Green Video (75 ohm, 0.7 V p-p)
3	BLUE	NEW	Blue Video (75 ohm, 0.7 V p-p)
4	RES	-	Reserved
5	GND	NEW	Ground
6	RGND	NEW	Red Ground
7	GGND	NEW	Green Ground
8	BGND	NEW	Blue Ground
9	+5V	NEW	+5 VDC
10	SGND	NEW	Sync Ground
11	ID0	NEW	Monitor ID Bit 0 (optional)
12	SDA	NEW	DDC Serial Data Line
13	HSYNC or CSYNC	NEW	Horizontal Sync (or Composite Sync)
14	VSYNC	NEW	Vertical Sync
15	SCL	NEW	DDC Data Clock Line

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source:?

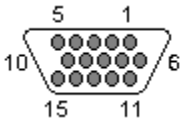
Please send any comments to Joakim Ogren.

VGA (15) Connector

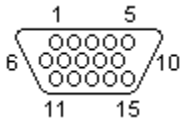
NEW
NEW
NEW

VGA (15)

VGA=Video Graphics Adapter or Video Graphics Array.
Videotype: Analogue.



(At the videocard)



(At the monitor cable)

15 PIN HIGHDENSITY D-SUB FEMALE at the videocard.
15 PIN HIGHDENSITY D-SUB MALE at the monitor cable.

Pin	Name	Dir	Description
1	RED	NEW	Red Video (75 ohm, 0.7 V p-p)
2	GREEN	NEW	Green Video (75 ohm, 0.7 V p-p)
3	BLUE	NEW	Blue Video (75 ohm, 0.7 V p-p)
4	ID2	NEW	Monitor ID Bit 2
5	GND	NEW	Ground
6	RGND	NEW	Red Ground
7	GGND	NEW	Green Ground
8	BGND	NEW	Blue Ground
9	KEY	-	Key (No pin)
10	SGND	NEW	Sync Ground
11	ID0	NEW	Monitor ID Bit 0
12	ID1 or SDA	NEW	Monitor ID Bit 1
13	HSYNC or CSYNC	NEW	Horizontal Sync (or Composite Sync)
14	VSYNC	NEW	Vertical Sync
15	ID3 or SCL	NEW	Monitor ID Bit 3

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

VGA (9) Connector

NEW
NEW
NEW

VGA (9)

VGA=Video Graphics Adapter or Video Graphics Array.
Videotype: Analogue.

NEW (At the videocard)

NEW (At the monitor cable)

9 PIN D-SUB FEMALE at the videocard.
9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Dir	Description
1	RED	NEW	Red Video
2	GREEN	NEW	Green Video
3	BLUE	NEW	Blue Video
4	HSYNC	NEW	Horizontal Sync
5	VSYNC	NEW	Vertical Sync
6	RGND	-	Red Ground
7	GGND	-	Green Ground
8	BGND	-	Blue Ground
9	SGND	-	Sync Ground

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

CGA Connector

NEW
NEW
NEW

CGA

CGA=Color Graphics Adapter.
Videotype: TTL, 16 colors.
Also known as IBM RGBI.

NEW (At the videocard)

NEW (At the monitor cable)
9 PIN D-SUB FEMALE at the videocard.
9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	R	Red
4	G	Green
5	B	Blue
6	I	Intensity
7	RES	Reserved
8	HSYNC	Horizontal Sync
9	VSYNC	Vertical Sync

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

EGA Connector

NEW
NEW
NEW

EGA

EGA=Enhanced Graphics Adapter.
Videotype: TTL, 16/64 colors.

NEW (At the videocard)

NEW (At the monitor cable)
9 PIN D-SUB FEMALE at the videocard.
9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	GND	Ground
2	SR	Secondary Red
3	PR	Primary Red
4	PG	Primary Green
5	PB	Primary Blue
6	SG/I	Secondary Green / Intensity
7	SB	Secondary Blue
8	H	Horizontal Sync
9	V	Vertical Sync

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

PGA Connector

NEW
NEW
NEW

PGA

Videotype: Analogue.

NEW (At the videocard)

NEW (At the monitor cable)

9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	R	Red
2	G	Green
3	B	Blue
4	CSYNC	Composite Sync
5	MODE	Mode Control
6	RGND	Red Ground
7	GGND	Green Ground
8	BGND	Blue Ground
9	GND	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

MDA (Hercules) Connector

NEW
NEW
NEW

MDA (Hercules)

NEW (At the videocard)

NEW (At the monitor cable)
9 PIN D-SUB FEMALE at the videocard.
9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	n/c	
4	n/c	
5	n/c	
6	I	Intensity
7	M	Mono Video
8	H	Horizontal Sync
9	V	Vertical Sync

Contributor: Joakim Ogren

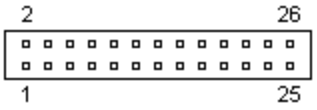
Source:?

Please send any comments to Joakim Ogren.

VGA Feature Connector

NEW
NEW
NEW

VGA Feature



(At the videocard)

26 PIN IDC at the Video card.

Pin	Name	Description
1	PD0	DAC Pixel Data Bit 0 (PB)
2	PD1	DAC Pixel Data Bit 1 (PG)
3	PD2	DAC Pixel Data Bit 2 (PR)
4	PD3	DAC Pixel Data Bit 3 (PI)
5	PD4	DAC Pixel Data Bit 4 (SB)
6	PD5	DAC Pixel Data Bit 5 (SG)
7	PD6	DAC Pixel Data Bit 6 (SR)
8	PD7	DAC Pixel Data Bit 7 (SI)
9	CLK	DAC Clock
10	BLK	DAC Blanking
11	HSYNC	Horizontal Sync
12	VSYNC	Vertical Sync
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17		Select Internal Video
18		Select Internal Sync
19		Select Internal Dot Clock
20	n/c	Not used
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	n/c	Not used
26	n/c	Not used

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Macintosh Video Connector

NEW
NEW
NEW

Macintosh Video

NEW (At the Computer)

15 PIN D-SUB ??? at the Computer.

Pin	Name	Dir	Description
1	RGND	NEW	Red Ground
2	R	NEW	Red
3	CSYNC	NEW	Composite sync
4	SENSE0	NEW	Monitor Sense 0
5	G	NEW	Green
6	GGND	NEW	Green Ground
7	SENSE1	NEW	Monitor Sense 1
8	n/c	-	No connection
9	B	NEW	Blue
10	SENSE2	NEW	Monitor sense 2
11	SGND	NEW	Sync Ground
12	VSYNC	NEW	Vertical Sync
13	BGND	NEW	Blue Ground
14	HSYNCGND	NEW	Horizontal Sync Ground
15	HSYNC	NEW	Horizontal Sync

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

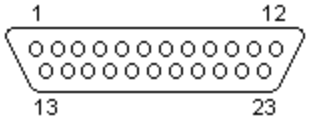
Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

Amiga Video Connector

NEW
NEW
NEW

Amiga Video



(At the Amiga)

23 PIN D-SUB MALE at the Amiga.

Pin	Name	Dir	Description
1	/XCLK	NEW	Extern Clock
2	/XCLKEN	NEW	Extern Clock Enable (47 Ohm)
3	RED	NEW	Analog Red (75 Ohm)
4	GREEN	NEW	Analog Green (75 Ohm)
5	BLUE	NEW	Analog Blue (75 Ohm)
6	DI	NEW	Digital Intensity (47 Ohm)
7	DR	NEW	Digital Red (47 Ohm)
8	DG	NEW	Digital Green (47 Ohm)
9	DB	NEW	Digital Blue (47 Ohm)
10	/CSYNC	NEW	Composite Sync (47 Ohm)
11	/HSYNC	NEW	Horizontal Sync (47 Ohm)
12	/VSYNC	NEW	Vertical Sync (47 Ohm)
13	GNDRTN	-	Digital Ground (for /XCLKEN) Don't connect with pin 16-20.
14	/PIXELSW	NEW	Genlock overlay (47 Ohm)
15	/C1	NEW	Clock out (47 Ohm)
16	GND	-	Video Ground
17	GND	-	Video Ground
18	GND	-	Video Ground
19	GND	-	Video Ground
20	GND	-	Video Ground
21	-12V	-	-12 Volts DC (10 mA max) (A500/A600/A1200)
	-5V	-	-5 Volts DC (10 mA max) (A1000/A2000/A3000/A4000)
22	+12V	-	+12 Volts DC (100 mA max)
23	+5V	-	+5 Volts DC (100 mA max)

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

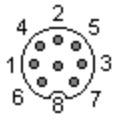
Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

Amiga 1000 RF Monitor Connector

NEW
NEW
NEW

Amiga 1000 RF Monitor



(At the computer)

8 PIN DIN "C" FEMALE at the computer.

Pin	Name	Dir	Description
1	n/c	-	Not connected
2	GND	NEW	Ground
3	AUDL	NEW	Audio Left
4	CVIDEO	NEW	Composite Video
5	GND	NEW	Ground
6	n/c	-	Not connected
7	+12V	NEW	+12 VDC
8	AUDR	NEW	Audio Right

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

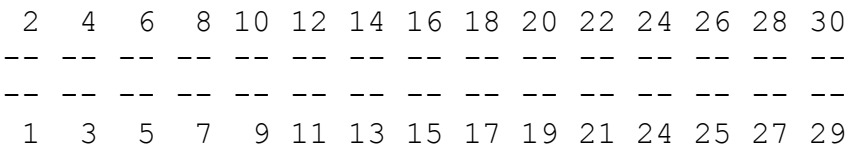
Source:?

Please send any comments to Joakim Ogren.

CDTV Video Slot Connector

NEW
NEW
NEW

CDTV Video Slot



NEW (At the computer)

30 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	GND	Video Ground
2	GND	Video Ground
3	XCLK	External Genlock Clock (in)
4	R	Red (in to video card)
5	/XCLKEN	Enables External Clock on XCLK.
6	BR	Buffered Red (out from video card)
7	GND	Video Ground
8	G	Green (in to video card)
9	GMS0	Genlock mode 0 (from computer, genlock button)
10	BG	Buffered Green (out from video card)
11	GMS1	Genlock mode 1 (from computer, genlock button)
12	B	Blue (in to video card)
13	/PIXELSW	Genlock signal
14	BB	Buffered Blue (out from video card)
15	VSYNC	Vertical Sync (in to video card)
16	CSYNC	Horizontal Sync (in to video card)
17	HSYNC	Composite Sync (in to video card)
18	BCSYNC	Buffered Composite Sync (out from video card)
19	GND	Video Ground
20	AUDR	Audio Right Output (from computer to RF modulator)
21	DGND	Digital Ground
22	AUDL	Audio Left Output (from computer to RF modulator)
23	-12V	-12 VDC (can be -5 VDC instead)
24	DGND	Digital Ground
25	+12V	+12 VDC
26	/CD/TV	CD/TV button. (Low=CDTV video on RF, High=Antenna)
27	VCC	+5 VDC
28	/CCK	3.58 MHz color clock (C1 clock)
29	GND	Video Ground
30	VCC	+5 VDC

Note: Used for RF-modulator usually.

Contributor: Joakim Ogren

Source:Darren Ewaniuk's CDTV Technical Information

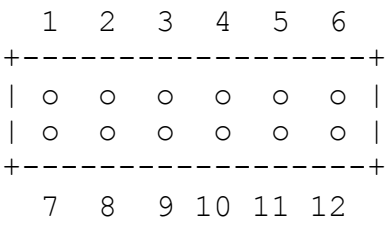
Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://nyquist.ee.ualberta.ca/~ewaniu/cdtv/cdtv-technical.html
Open this address in your WWW browser.

PlayStation A/V Connector

NEW
NEW
NEW

PlayStation A/V



NEW (At the PlayStation)

12 PIN ?? at the PlayStation.

Pin	Name	Description
1	?	
2	?	
3	?	
4	?	
5	B	Blue
6	R	Red
7	?	
8	AR	Right Audio
9	CSYNC	Composite Sync
10	VGND	Video Ground
11	?	
12	G	Green

Contributor: Joakim Ogren

Source:Sony PlayStation FAQ

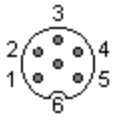
Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.gla.ac.uk/~gkrx11/PSX/FAQ.html
Open this address in your WWW browser.

Commodore 1084 & 1084S (Analog) Connector

NEW
NEW
NEW

Commodore 1084 & 1084S (Analog)



(At the Monitor)

6 PIN DIN FEMALE at the Monitor.

Pin	Name	Description
1	G	Green
2	HSYNC	Horizontal Sync
3	GND	Ground
4	R	Red
5	B	Blue
6	VSYNC	Vertical Sync

Contributor: Joakim Ogren

Source:National Amiga's C1084 page

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.interlog.com/~gscott/t-1084.html
Open this address in your WWW browser.

Commodore 1084 & 1084S (Digital) Connector

NEW
NEW
NEW

Commodore 1084 & 1084S (Digital)

NEW (At the Monitor)

8 PIN DIN 'C' FEMALE at the Monitor.

Pin	Name	Description
1	n/c	Not connected
2	R	Red
3	G	Green
4	B	Blue
5	I	Intensity
6	GND	Ground
7	HSYNC	Horizontal Sync
8	VSYNC	Vertical Sync

Contributor: Joakim Ogren

Source:National Amiga's C1084 page

Please send any comments to Joakim Ogren.

Commodore 1084d & 1084dS Connector

NEW
NEW
NEW

Commodore 1084d & 1084dS

NEW (At the Monitor)

9 PIN D-SUB MALE ?? at the Monitor.

Pin	Name	Analog Mode	Digital Mode
1	GND	Ground	Ground
2	GND	Ground	Ground
3	R	Red	Red
4	G	Green	Green
5	B	Blue	Blue
6	I	n/c	Intensity
7	CSYNS	Composite Sync	n/c
8	HSYNC	n/c	Horizontal Sync
9	VSYNC	n/c	Vertical Sync

Contributor: Joakim Ogren

Source:National Amiga's C1084d page

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.interlog.com/~gscott/t-1084d.html
Open this address in your WWW browser.

Atari Jaguar A/V Connector

NEW
NEW
NEW

Atari Jaguar A/V

```
                    TOP (duh)

1A   2A   3A   4A   5A   6A   7A   8A   9A   10A   11A   12A

1B   2B   3B   4B   5B   6B   7B   8B   9B   10B   11B   12B
```

NEW (At the Atari)

12 PIN ?? at the Atari.

Pin	Name	Description
1A	AL	Audio Left
2A	AGND	Audio Ground
3A	GND	Ground
4A	GND (chroma)	Ground (Chroma)
5A	B	RGB Blue
6A	HSYNC	Horizontal sync
7A	G	RGB Green
8A	CHROMA	Chroma
9A	GND ???	Ground ???
10A	+5V ???	+5 VDC ???
11A	+5V ???	+5 VDC ???
12A	?	?
1B	AR	Right audio
2B	AGND	Audio GND
3B	GND	Ground
4B	R	RGB Red
5B	CSYNC	Composite (Vertical) Sync
6B	?	?
7B	LGND	Luminance Ground
8B	LUM	Luminance
9B	GND	Ground
10B	CVBSGND	Composite Video Ground
11B	CVBS	Composite Video
12B	?	?

Contributor: Joakim Ogren

Source:Scooping out Jaguar RGB by Duncan Brown in Atari Explorer Online Vol.3 Issue 6

Please send any comments to Joakim Ogren.

This the e-mail address:
BROWN_DU@Eisner.DECUS.Org
Choose this address in your e-mail reader.

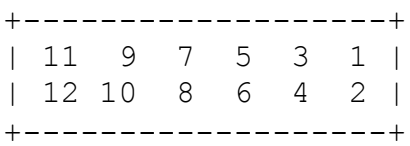
This is the URL for the WWW page:
http://www.redsun.net/jaguar/aeo/aeo_0306.txt
Open this address in your WWW browser.

SNES Video Connector

NEW
NEW
NEW

SNES Video

Availble on the Nintendo SNES.



NEW (At the SNES)
UNKNOWN CONNECTOR at the SNES.

Pin	Name	Description
1	R	Red (Requires 200 uF in serie)
2	G	Green (Requires 200 uF in serie)
3	CSYNC	Composite Sync
4	B	Blue (Requires 200 uF in serie)
5	GND	Ground
6	GND	Ground
7	Y	S-Video Y
8	C	S-Video C
9	CVBS	Composite Video (NTSC)
10	+5V	+5 VDC
11	L+R	Left+Right Audio (Mono)
12	L-R	Left-Right Audio (Used to calculate Stereo)

Contributor: Joakim Ogren

Source:Video Games FAQ (Part 3), Pinout from Radio Electronics April 1992

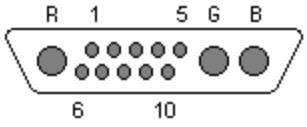
Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.lib.ox.ac.uk/internet/news/faq/archive/games.video-games.faq.part3.html
Open this address in your WWW browser.

Sun Video Connector

NEW
NEW
NEW

Sun Video



(At the Computer)

13 PIN 13W3 FEMALE at the Computer.

Pin	Name	Description
1	GND	Ground*
2	VSYNC	Vertical Sync*
3	SENSE2	Sense #2
4	SENSEGND	Sense Ground
5	CSYNC	Composite Sync
6	HSYNC	Horizontal Sync*
7	GND	Ground*
8	SENSE1	Sense #1
9	SENSE0	Sense #0
10	CGND	Composite Ground
R	RED	Red
G	GREEN/GRAY	Green/Gray
B	BLUE	Blue

*) Considered obsolete, may not be connected.

Monitor-sense bits defined as:

Value	Bit 2	Bit 1
0	0	0
1	0	0
2	0	1
3	0	1
4	1	0
5	1	0
6	1	1
7	1	1

See http://cvs.anu.edu.au:80/monitorconversion/ and http://rugmd0.chem.rug.nl/~everdij/hitachi.html for info on attaching old workstation monitors to VGA boards.

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://cvs.anu.edu.au:80/monitorconversion/
Open this address in your WWW browser.

This is the URL for the WWW page:
http://rugmd0.chem.rug.nl/~everdij/hitachi.html
Open this address in your WWW browser.

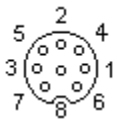
ZX Spectrum 128 RGB Connector

NEW
NEW
NEW

ZX Spectrun 128 RGB

Can be found at the Sinclair ZX Spectrum 128.

NEW (At the computer)



(At the monitor cable)

8 PIN DIN (DIN45326) FEMALE at the computer.

8 PIN DIN (DIN45326) MALE at the monitor cable.

Pin	Name	Dir	Description
1	CVBS	NEW	Composite Video (PAL, 75 ohms, 1.2V p-p)
2	GND	NEW	Ground
3	BOUT	NEW	Bright Output
4	CSYNC	NEW	Composite Sync
5	VSYNC	NEW	Vertical Sync
6	G	NEW	Green
7	R	NEW	Red
8	B	NEW	Blue

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source:Online ZX Spectrum 128 Manual Page 3

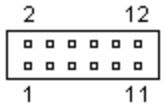
Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://users.ox.ac.uk/~uzdm0006/Damien/speccy/128manua/sp128p03.html
Open this address in your WWW browser.

3b1/7300 Video Connector

NEW
NEW
NEW

3b1/7300 Video



(At the computer)

12 PIN IDC MALE at the computer.

Pin	Name	Description
1	VSYNC	Vertical Sync
2	GND	Ground
3	HSYNC	Horizontal Sync
4	GND	Ground
5	VIDEO	Video
6	GND	Ground
7	+12V	+12 VDC
8	GND	Ground
9	+12V	+12 VDC
10	SPK	Speaker
11	SPK	Speaker
12	?	?

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

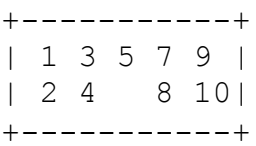
Please send any comments to Joakim Ogren.

CM-8/CoCo RGB Connector

NEW
NEW
NEW

CM-8/CoCo RGB

Availble on the Tandy/Radio Shack Color Computer (CoCo).



NEW (At the CoCo)
UNKNOWN CONNECTOR at the CoCo.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	R	Red
4	G	Green
5	B	Blue
6	KEY	No Pin
7	AUDIO	Audio
8	HSYNC	Horizontal Sync
9	VSYNC	Vertical Sync
10	n/c	No Connection

Contributor: Joakim Ogren

Source:Tandy Color Computer FAQ at Video Game Advantage's homepage

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.io.com/~vga2000/faqs/coco.faq
Open this address in your WWW browser.

This is the URL for the WWW page:
http://www.io.com/~vga2000/
Open this address in your WWW browser.

AT&T 53D410 Connector

NEW
NEW
NEW

AT&T 53D410

NEW (At the computer)
25 PIN D-SUB ??? at the computer.

Pin	Name	Description
1	?	?
2	VSYNC	Vertical Sync
3	HSYNC	Horizontal Sync
4	?	?
5	VIDEO	Video
6	?	?
7	?	?
8	?	?
9	?	?
10	?	?
11	?	?
12	?	?
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	?	?
17	?	?
18	?	?
19	?	?
20	?	?
21	?	?
22	?	?
23	?	?
24	?	?
25	?	?

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

AT&T 6300 Taxan Monitor Connector

NEW
NEW
NEW

AT&T 6300 Taxan Monitor

NEW (At the Monitor)

8 PIN DIN (DIN45326) FEMALE at the Monitor.

Pin	Name	Description
1	TEXT	Special TEXT signal (??)
2	R	Red
3	G	Green
4	B	Blue
5	I	Intensity
6	GND	Signal Ground
7	HSYNC/CSYNC	Horizontal or Composite Sync
8	VSYNC	Vertical Sync

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

AT&T PC6300 Connector

NEW
NEW
NEW

AT&T PC6300

NEW (At the computer)
25 PIN D-SUB ??? at the computer.

Pin	Name	Description
1	HSYNC	Horizontal Sync
2	ID0	Monitor ID 0
3	VSYNC	Vertical Sync
4	R	Red
5	G	Green
6	B	Blue
8	n/c	Not connected
9	n/c	Not connected
10	ID1	Monitor ID 1
11	MODE0	Mode 0
12	n/c	Not connected
13	/DEGAUSS	Degauss
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	n/c	Not connected
23	n/c	Not connected
24	+15V	+15 VDC
25	+15V	+15 VDC

Monochrome monitor: ID0 and ID1 are open
Color monitor: ID0 is 0, and ID1 is 1, probably 5V, not 15V

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

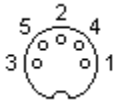
Please send any comments to Joakim Ogren.

Vic 20 Video Connector

NEW
NEW
NEW

Vic 20 Video

(At the computer)



(At the cable)

5 PIN DIN 180~ (DIN41524) FEMALE at the Computer.
5 PIN DIN 180~ (DIN41524) MALE at the Cable.

Pin	Name	Dir	Description
1	+6V	NEW	+6 VDC (10 mA max)
2	GND	NEW	Ground
3	AUDIO	NEW	Audio
4	VLOW	NEW	Video Low (Unconnected ?)
5	VHIGH	NEW	Video High

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source: CBM Memorial Page Pinouts

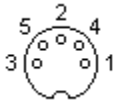
Please send any comments to Joakim Ogren.

C64 Audio/Video Connector

NEW
NEW
NEW

C64 Audio/Video

(At the computer)



(At the cable)

5 PIN DIN 180~ (DIN41524) FEMALE at the Computer.
5 PIN DIN 180~ (DIN41524) MALE at the Cable.

Pin	Name	Dir	Description
1	LUM	NEW	Luminance
2	GND	NEW	Ground
3	AOUT	NEW	Audio Out
4	VOUT	NEW	Video Out
5	AIN	NEW	Audio In

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

C65 Video Connector

NEW
NEW
NEW

C65 Video

Availble on the Commodore C65 computer.

NEW (At the Computer)

9 PIN D-SUB MALE at the Computer.

Pin	Name	Dir	Description
1	GND	NEW	Ground
2	?		?
3	R	NEW	Red
4	G	NEW	Green
5	B	NEW	Blue
6	?		?
7	CSYNC	NEW	Composite Sync
8	HSYNC	NEW	Horizontal Sync
9	VSYNC	NEW	Vertical Sync

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source: CBM Memorial Page Pinouts

Please send any comments to Joakim Ogren.

C128 RGBI Connector

NEW
NEW
NEW

C128 RGBI

NEW (At the Computer)

9 PIN D-SUB FEMALE at the Computer.

Pin	Name	Dir	Description
1	GND	NEW	Ground
2	GND	NEW	Ground
3	R	NEW	Red
4	G	NEW	Green
5	B	NEW	Blue
6	I	NEW	Intensity
7	VIDEO	NEW	Composite Video
8	HSYNC	NEW	Horizontal Sync
9	VSYNC	NEW	Vertical Sync

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source: Usenet posting in comp.sys.cbm, C128 screen cables by Marko Makela

Please send any comments to Joakim Ogren.

This the e-mail address:
msmakela@cc.helsinki.fi
Choose this address in your e-mail reader.

C128/C64C Video Connector

NEW
NEW
NEW

C128/C64C Video

Seems to be availble on the C128 and the C64C (white colour). Compatible with cables for the 5 pin D-SUB on C64's.

NEW (At the Computer)
8 PIN DIN (DIN45326) FEMALE at the Computer.

Pin	Name	Dir	Description
1	LUM	NEW	Luminance (monochrome video)
2	GND	NEW	Ground
3	AOUT	NEW	Audio out
4	VOUT	NEW	Composite Video out
5	AIN	NEW	Audio in (into the SID chip)
6	n/c	-	Not connected
7	n/c	-	Not connected
8	C	NEW	Chroma

Note: Direction is Computer relative Monitor.

Contributor: Joakim Ogren

Source: CBM Memorial Page Pinouts

Please send any comments to Joakim Ogren.

CBM 1902A Connector

NEW
NEW
NEW

CBM 1902A

Availble on the Commodore CBM 1902A monitor.

NEW (At the Monitor)

6 PIN DIN FEMALE at the Monitor.

Pin	Name	Dir	Description
1	n/c	-	Not connected
2	AUDIO	NEW	Audio
3	GND	NEW	Ground
4	C	NEW	Chroma
5	n/c	-	Not connected
6	L	NEW	Luminance

Note: Direction is Monitor relative Computer.

Contributor: Joakim Ogren

Source: comp.sys.cbm General FAQ v3.1 Part 7

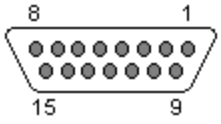
Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.lib.ox.ac.uk/internet/news/faq/archive/cbm-main-faq.3.1.p7.html
Open this address in your WWW browser.

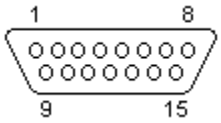
PC Gameport Connector

NEW
NEW
NEW

PC Gameport



(At the computer)



(At the joystick cable)

15 PIN D-SUB FEMALE at the computer.
15 PIN D-SUB MALE at the joystick cable.

Pin	Name	Dir	Description
1	+5V	NEW	+5 VDC
2	/B1	NEW	Button 1
3	X1	NEW	Joystick 1 - X
4	GND	NEW	Ground
5	GND	NEW	Ground
6	Y1	NEW	Joystick 1 - Y
7	/B2	NEW	Button 2
8	+5V	NEW	+5 VDC
9	+5V	NEW	+5 VDC
10	/B4	NEW	Button 4
11	X2	NEW	Joystick 2 - X
12	GND	NEW	Ground
13	Y2	NEW	Joystick 2 - Y
14	/B3	NEW	Button 3
15	+5V	NEW	+5 VDC

Note: Direction is Computer relative Joystick.
Note: Use 100kohm resistor.

Contributor: Joakim Ogren

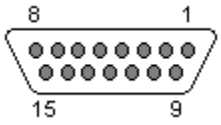
Source:?

Please send any comments to Joakim Ogren.

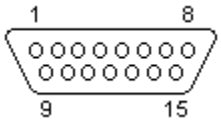
NEW
NEW
NEW

PC Gameport+MIDI

Some soundcards have some MIDI signals included in their Gameport. Ground and VCC has been used for this.



(At the computer)



(At the joystick cable)

15 PIN D-SUB FEMALE at the computer.
15 PIN D-SUB MALE at the joystick cable.

Pin	Name	Dir	Description
1	+5V	NEW	+5 VDC
2	/B1	NEW	Button 1
3	X1	NEW	Joystick 1 - X
4	GND	NEW	Ground
5	GND	NEW	Ground
6	Y1	NEW	Joystick 1 - Y
7	/B2	NEW	Button 2
8	+5V	NEW	+5 VDC
9	+5V	NEW	+5 VDC
10	/B4	NEW	Button 4
11	X2	NEW	Joystick 2 - X
12	MIDITXD	NEW	MIDI Transmit
13	Y2	NEW	Joystick 2 - Y
14	/B3	NEW	Button 3
15	MIDIRXD	NEW	MIDI Recieve

Note: Direction is Computer relative Joystick.
Note: Use 100kohm resistor.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Amiga Mouse/Joy Connector

NEW
NEW
NEW

Amiga Mouse/Joy

NEW (At the computer)

NEW (At the mouse/joy cable)
9 PIN D-SUB MALE at the computer.
9 PIN D-SUB FEMALE at the mouse/joy cable.

Pin	Mouse/Trackball	Lightpen	Digital Joystick	Paddle	Dir	Comment
1	V-pulse	n/c	/FORWARD	BUTTON 3	NEW	
2	H-pulse	n/c	/BACK	n/c	NEW	
3	VQ-pulse	n/c	/LEFT	BUTTON 1	NEW	
4	HQ-pulse	n/c	/RIGHT	BUTTON 2	NEW	
5	BUTTON 3(M)	Penpress	n/c	PotX	NEW	
6	BUTTON 1(L)	/Beamtrigger	/BUTTON 1	n/c	NEW	
7	+5V	+5V	+5V	+5V	NEW	50 mA max
8	GND	GND	GND	GND	NEW	
9	BUTTON 2(R)	BUTTON 2	BUTTON 2	PotY	NEW	

Note: Direction is Computer relative Device.
Note: Pot is a linear 470 kOhm (+/-10 %)

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

MSX Joystick Connector

NEW
NEW
NEW

MSX Joystick

NEW (At the computer)

NEW (At the joystick cable)
9 PIN D-SUB MALE at the computer.
9 PIN D-SUB FEMALE at the joystick cable.

Pin	Name	Dir	Description
1	/FORWARD	NEW	Forward
2	/BACK	NEW	Backward
3	/LEFT	NEW	Left
4	/RIGHT	NEW	Right
5	+5V	NEW	+5 VDC (50mA max)
6	/TRG1	NEW	Trigger A / Output 1
7	/TRG2	NEW	Trigger A / Output 1
8	OUTPUT	NEW	Output 3
9	GND	NEW	Signal Ground

Note: Direction is Computer relative Joystick.

Warning: Pin 5 is +5V on MSX and Mouse Button 2 on Amiga. Since Amiga mousebutton is active low, connecting an Amiga mouse to a MSX and pressing mousebutton 2 will shortcut the supply voltage.

Contributor: Joakim Ogren

Source:Mayer's SV738 X'press I/O map

Please send any comments to Joakim Ogren.

SGI Mouse (Model 021-0004-002) Connector

NEW
NEW
NEW

SGI Mouse (Model 021-0004-002)

NEW (At the Computer)

9 PIN D-SUB ??? at the Computer.

Pin	Name	Dir	Description
1	+5V	NEW	+5 VDC
2	-5V	NEW	-5 VDC
3	n/c	-	Not connected
4	n/c	-	Not connected
5	MTXD	NEW	Data
6	n/c	-	Not connected
7	n/c	-	Not connected
8	n/c	-	Not connected
9	GND	NEW	Ground

Note: Direction is Computer relative Mouse.

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

Atari Enhanced Joystick Connector

NEW
NEW
NEW

Atari Enhanced Joystick

Can be found at Atari Falcon, Jaguar & STe.

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	UP0	Up 0
2	DOWN0	Down 0
3	LEFT0	Left 0
4	RIGHT0	Right 0
5	PAD0Y	Paddle 0 Y
6	FIRE0/LIGHT GUN	Fire 0/Lightgun
7	VCC	+5 VDC
8	n/c	Not connected
9	GND	Ground
10	FIRE2	Fire 2
11	UP2	Up 2
12	DOWN2	Down 2
13	LEFT2	Left 2
14	RIGHT2	Right 2
15	PAD0X	Paddle 0 X

Contributor: Joakim Ogren

Source:Do-It-Yourself Atari Jaguar Controller by Andrew Hague

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://dcpu1.cs.york.ac.uk:6666/~andrew/atari/DIYjoypad.txt
Open this address in your WWW browser.

This the e-mail address:
andrew@minster.york.ac.uk
Choose this address in your e-mail reader.

Atari 2600 Joystick Connector

NEW
NEW
NEW

Atari 2600 Joystick

NEW (At the Atari)

NEW (At the joystick cable)

9 PIN D-SUB MALE at the Atari.

9 PIN D-SUB FEMALE at the joystick cable.

Pin	Color	Dir	Description
1	WHT	NEW	Up
2	BLU	NEW	Down
3	GRN	NEW	Left
4	BRN	NEW	Right
5	n/c	-	Not connected
6	ORG	NEW	Button
7	n/c	-	Not connected
8	BLK	NEW	Ground(-)
9	n/c	-	Not connected

Note: Direction is Computer relative Joystick.
Note: Connect Direction/Button to Ground for action.

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ, Pinout by Greg Alt

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.dhp.com/~sloppy/files/classic/atari/atari.faq
Open this address in your WWW browser.

This the e-mail address:

galt@cs.utah.edu

Choose this address in your e-mail reader.

Atari 6200 Joystick Connector

NEW
NEW
NEW

Atari 6200 Joystick

NEW (At the Atari)
UNKNOWN CONNECTOR at the Atari.

Pin	Description
1	Keypad -- right column
2	Keypad -- middle column
3	Keypad -- left column
4	Start, Pause, and Reset common
5	Keypad -- third row and Reset
6	Keypad -- second row and Pause
7	Keypad -- top row and Start
8	Keypad -- bottom row
9	Pot common
10	Horizontal pot (POT0, 2, 4, 6)
11	Vertical pot (POT1, 3, 5, 7)
12	5 volts DC
13	Bottom side buttons (TRIG0, 1, 2, 3)
14	Top side buttons
15	0 volts -- ground

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ

Please send any comments to Joakim Ogren.

Atari 7800 Joystick Connector

NEW
NEW
NEW

Atari 7800 Joystick

NEW (At the Atari)

NEW (At the joystick cable)

9 PIN D-SUB MALE at the Atari.

9 PIN D-SUB FEMALE at the joystick cable.

Pin	Color	Dir	Description
1	WHT	NEW	Up
2	BLU	NEW	Down
3	GRN	NEW	Left
4	BRN	NEW	Right
5	RED	NEW	Button (R)ight (-)
6	ORG	?	Both buttons (+)
7	n/c	-	Not connected
8	BLK	NEW	Ground(-)
9	YLW	NEW	Button (L)eft (-)

Note: Direction is Computer relative Joystick.

Note: Connect Direction and Button(L/R) to Ground for action. And Both Button to Button L and Button R for action.

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ

Please send any comments to Joakim Ogren.

Keyboard (5 PC) Connector

NEW
NEW
NEW

Keyboard (5 PC)

NEW (At the computer)

5 PIN DIN 180~ (DIN41524) FEMALE at the computer.

Pin	Name	Description	Technical
1	CLOCK	Clock	CLK/CTS, Open-collector
2	DATA	Data	RxD/TxD/RTS, Open-collector
3	n/c	Not connected	Reset on some very old keyboards.
4	GND	Ground	
5	VCC	+5 VDC	

Contributor: Joakim Ogren

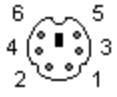
Source:?

Please send any comments to Joakim Ogren.

Keyboard (6 PC) Connector

NEW
NEW
NEW

Keyboard (6 PC)



(At the computer)

6 PIN MINI-DIN FEMALE (PS/2 STYLE) at the computer.

Pin	Name	Dir	Description
1	DATA	NEW	Key Data
2	n/c	-	Not connected
3	GND	NEW	Gnd
4	VCC	NEW	Power , +5 VDC
5	CLK	NEW	Clock
6	n/c	-	Not connected

Note: Direction is Computer relative Keyboard.

Contributor: Joakim Ogren, Gilles Ries

Source:?

Please send any comments to Joakim Ogren.

This the e-mail address:

gries@glo.be

Choose this address in your e-mail reader.

Keyboard (XT) Connector

NEW
NEW
NEW

Keyboard (XT)

NEW (At the computer)
5 PIN DIN 180~ (DIN41524) FEMALE at the computer.

Pin	Name	Description	Technical
1	CLK	Clock	CLK/CTS, Open-collector
2	DATA	Data	RxD, Open-collector
3	/RESET	Reset	
4	GND	Ground	
5	VCC	+5 VDC	

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Keyboard (5 Amiga) Connector

NEW
NEW
NEW

Keyboard (5 Amiga)

NEW (At the computer)

5 PIN DIN 180~ (DIN41524) FEMALE (A1000/A2000/A3000) at the computer.

Pin	A1000	A2000/A3000
1	+5 Volts	KCLK
2	CLOCK	KDAT
3	DATA	n/c
4	GND	GND
5		+5 Volts

Contributor: Joakim Ogren

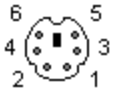
Source:?

Please send any comments to Joakim Ogren.

Keyboard (6 Amiga) Connector

NEW
NEW
NEW

Keyboard (6 Amiga)



(At the computer)

6 PIN MINI-DIN FEMALE (PS/2 STYLE) (A4000/CD32/CDTV) at the computer.

Pin	Name	Dir	Description
1	DATA	NEW	Data
2	n/c	-	Not connected
3	GND	NEW	Ground
4	+5V	NEW	+5 Volts DC (100 mA max)
5	CLOCK	NEW	Clock
6	n/c	-	Not connected

Note: Direction is Computer relative Keyboard.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

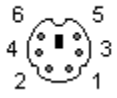
Please send any comments to Joakim Ogren.

Keyboard (Amiga CD32) Connector

NEW
NEW
NEW

Keyboard (Amiga CD32)

The Amiga CD32 keyboard connector also includdes a serialport.



(At the computer)

6 PIN MINI-DIN FEMALE (PS/2 STYLE) at the computer.

Pin	Name	Dir	Description
1	DATA	NEW	Data
2	/TxD	NEW	Transmit Data (0-5V and reversed)
3	GND	NEW	Ground
4	+5V	NEW	+5 Volts DC (100 mA max)
5	CLOCK	NEW	Clock
6	/RxD	NEW	Recieve Data (0-5V and reversed)

Note: Direction is Computer relative Keyboard.

Contributor: Joakim Ogren

Source:CD32 keyboard port info, usenet posting by Klaus Hegemann.

Please send any comments to Joakim Ogren.

This the e-mail address:
Klaus_Hegemann@punk.fido.de
Choose this address in your e-mail reader.

AT&T 6300 Keyboard Connector

NEW
NEW
NEW

AT&T 6300 Keyboard

NEW (At the Computer)

9 PIN D-SUB ??? at the Computer.

Pin	Name	Description
1	DATA	Data
2	CLOCK	Clock
3	GND	Ground
4	GND	Ground
5	+12V	+12 VDC
6	n/c	Not connected
7	n/c	Not connected
8	n/c	Not connected
9	n/c	Not connected

Contributor: Joakim Ogren

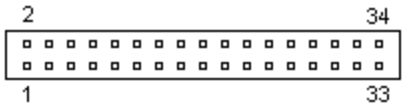
Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

Internal Diskdrive Connector

NEW
NEW
NEW

Internal Diskdrive



(At the computer & diskdrives)

34 PIN IDC MALE at the computer & diskdrives.

Pin	Name	Dir	Description
2	/REDWC	NEW	Density Select
4	n/c		Reserved
6	n/c		Reserved
8	/INDEX	NEW	Index
10	/MOTEA	NEW	Motor Enable A
12	/DRVSB	NEW	Drive Sel B
14	/DRVSA	NEW	Drive Sel A
16	/MOTEB	NEW	Motor Enable B
18	/DIR	NEW	Direction
20	/STEP	NEW	Step
22	/WDATE	NEW	Write Data
24	/WGATE	NEW	Floppy Write Enable
26	/TRK00	NEW	Track 0
28	/WPT	NEW	Write Protect
30	/RDATA	NEW	Read Data
32	/SIDE1	NEW	Head Select
34	/DSKCHG	NEW	Disk Change

Note: Direction is Computer relative Diskdrive.
Note: All odd pins are GND, Ground.

Note: Can be an Edge-connector on old PC's.

Contributor: Joakim Ogren

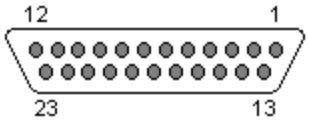
Source:?

Please send any comments to Joakim Ogren.

Amiga External Diskdrive Connector

NEW
NEW
NEW

Amiga External Diskdrive



(At the Amiga)

23 PIN D-SUB FEMALE at the Amiga.

Pin	Name	Dir	Description
1	/RDY	NEW	Disk Ready
2	/DKRD	NEW	Disk Read Data
3	GND	NEW	Ground
4	GND	NEW	Ground
5	GND	NEW	Ground
6	GND	NEW	Ground
7	GND	NEW	Ground
8	/MTRXD	OC	Disk Motor Control
9	/SEL2	OC	Select Drive 2
10	/DRES	OC	Disk Reset
11	/CHNG	NEW	Disk Removed From Drive-Latched Low
12	+5V	NEW	+5 Volts DC (250 mA max)
13	/SIDE	NEW	Select Disk Side (0=Upper, 1=Lower)
14	/WPRO	NEW	Disk is Write Protected
15	/TKO	NEW	Drive Head position over Track 0
16	/DKWE	OC	Disk Write Enable
17	/DKWD	OC	Disk Write Data
18	/STEP	OC	Step the Head-Pulse, First low, then high
19	DIR	OC	Select Head Direction (0=Inner, 1=Outer)
20	/SEL3	OC	Select Drive 3
21	/SEL1	OC	Select Drive 1
22	/INDEX	OC	Disk Index Pulse
23	+12V	NEW	+12 Volts DC (160 mA max, 540 mA surge

Note: Direction is Computer relative Diskdrive.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

Please send any comments to Joakim Ogren.

MSX External Diskdrive Connector

NEW
NEW
NEW

MSX External Diskdrive

NEW (At the Computer)

25 PIN D-SUB FEMALE at the Computer.

Pin	Name	Dir	Description
1	+12V	NEW	+12 VDC
2	+5V	NEW	+5 VDC
3	+5V	NEW	+5 VDC
4	/INDEX	NEW	Sector hole passed sensor.
5	/DSEL1	NEW	Drive Select 1
6	DIR	NEW	Direction (0=In, 1=Dir)
7	/STEP	NEW	Moves head 1 step in DIR direction.
8	WRITEDATA	NEW	Write Data
9	/WRITEGATE	NEW	Write Gate
10	/TRACK00	NEW	Head is over Track 00 (outermost track)
11	/WRITEPROTECT	NEW	Write protected disk (0=Write protected)
12	READDATA	NEW	Data read from diskette.
13	/SIDESELECT	NEW	Side Select (0=Side 1, 1=Side 0)
14	+12V	NEW	+12 VDC
15	+12V	NEW	+12 VDC
16	+5V	NEW	+5 VDC
17	/DSEL1	NEW	Select Drive 0
18	/MOTOR	NEW	Motor On
19	READY	NEW	Ready
20	GND	NEW	Ground
21	GND	NEW	Ground
22	GND	NEW	Ground
23	GND	NEW	Ground
24	GND	NEW	Ground
25	GND	NEW	Ground

Note: Direction is Computer relative Diskdrive.

Contributor: Joakim Ogren

Source:Mayer's SV738 X'press I/O map

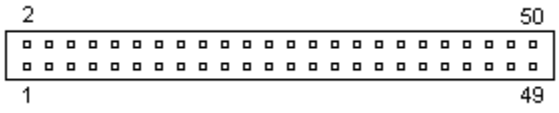
Please send any comments to Joakim Ogren.

SCSI Internal Connector

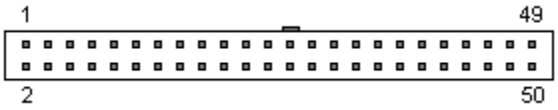
NEW
NEW
NEW

SCSI Internal

SCSI=Small Computer System Interface.
Based on an original design by Shugart Associates. SCSI was ratified in 1986.



(at the controller & harddisk)



(at the cable.)

50 PIN IDC MALE at the controller & harddisk.
50 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
2	DB0	NEW	Data Bus 0
4	DB1	NEW	Data Bus 1
6	DB2	NEW	Data Bus 2
8	DB3	NEW	Data Bus 3
10	DB4	NEW	Data Bus 4
12	DB5	NEW	Data Bus 5
14	DB6	NEW	Data Bus 6
16	DB7	NEW	Data Bus 7
18	PARITY	NEW	Data Parity (odd Parity)
20	GND	NEW	Ground
22	GND	NEW	Ground
24	GND	NEW	Ground
26	TMPWR	NEW	Termination Power
28	GND	NEW	Ground
30	GND	NEW	Ground
32	/ATN	NEW	Attention
34	GND	NEW	Ground
36	/BSY	NEW	Busy
38	/ACK	NEW	Acknowledge
40	/RST	NEW	Reset
42	/MSG	NEW	Message
44	/SEL	NEW	Select
46	/C/D	NEW	Control/Data
48	/REQ	NEW	Request
50	/I/O	NEW	Input/Output

Note: Direction is Device relative Bus (other Devices).

All odd-numbered pins, except pin 25, are connected to ground. Pin 25 is left open.

Contributor: Joakim Ogren

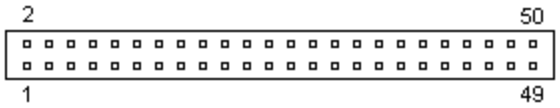
Source:?

Please send any comments to Joakim Ogren.

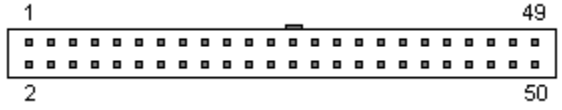
SCSI Internal Differential Connector

NEW
NEW
NEW

SCSI Internal Differential



(at the controller & harddisk.)



(at the cable.)

50 PIN IDC MALE at the controller & harddisk.
50 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
01	GND	NEW	Ground
02	GND	NEW	Ground
03	+DB0	NEW	+Data Bus 0
04	-DB0	NEW	-Data Bus 0
05	+DB1	NEW	+Data Bus 1
06	-DB1	NEW	-Data Bus 1
07	+DB2	NEW	+Data Bus 2
08	-DB2	NEW	-Data Bus 2
09	+DB3	NEW	+Data Bus 3
10	-DB3	NEW	-Data Bus 3
11	+DB4	NEW	+Data Bus 4
12	-DB4	NEW	-Data Bus 4
13	+DB5	NEW	+Data Bus 5
14	-DB5	NEW	-Data Bus 5
15	+DB6	NEW	+Data Bus 6
16	-DB6	NEW	-Data Bus 6
17	+DB7	NEW	+Data Bus 7
18	-DB7	NEW	-Data Bus Pariy7
19	+DBP	NEW	+Data Bus Parity (odd Parity)
20	-DBP	NEW	-Data Bus Pariy (odd Parity)
21	DIFFSENS	?	???
22	GND	NEW	Ground
23	res	-	Reserved
24	res	-	Reserved
25	TERMPWR	NEW	Termination Power
26	TERMPWR	NEW	Termination Power
27	res	-	Reserved
28	res	-	Reserved
29	+ATN	NEW	+Attention
30	-ATN	NEW	-Attention
31	GND	NEW	Ground
32	GND	NEW	Ground
33	+BSY	NEW	+Bus is busy
34	-BSY	NEW	-Bus is busy
35	+ACK	NEW	+Acknowledge

36	-ACK	NEW -Acknowledge
37	+RST	NEW +Reset
38	-RST	NEW -Reset
39	+MSG	NEW +Message
40	-MSG	NEW -Message
41	+SEL	NEW +Select
42	-SEL	NEW -Select
43	+C/D	NEW +Control or Data
44	-C/D	NEW -Control or Data
45	+REQ	NEW +Request
46	-REQ	NEW -Request
47	+I/O	NEW +In/Out
48	-I/O	NEW -In/Out
49	GND	NEW Ground
50	GND	NEW Ground

Note: Direction is Device relative Bus (other Devices).

Contributor: Joakim Ogren

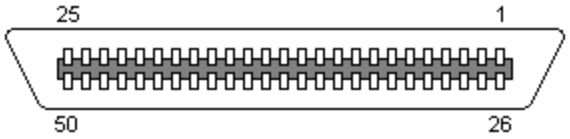
Source:?

Please send any comments to Joakim Ogren.

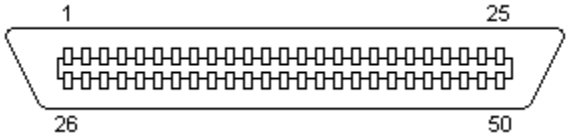
SCSI External Centronics 50 Connector

NEW
NEW
NEW

SCSI External Centronics 50



(At the controller & devices)



(At the cable)

50 PIN CENTRONICS FEMALE at the controller & devices.
50 PIN CENTRONICS MALE at the cable.

Pin	Name	Dir	Description
1-25	GND	NEW	Ground
26	DB0	NEW	Data Bus 0
27	DB1	NEW	Data Bus 1
28	DB2	NEW	Data Bus 2
29	DB3	NEW	Data Bus 3
30	DB4	NEW	Data Bus 4
31	DB5	NEW	Data Bus 5
32	DB6	NEW	Data Bus 6
33	DB7	NEW	Data Bus 7
34	PARITY	NEW	Data Parity (odd Parity)
35	GND	NEW	Ground
36	GND	NEW	Ground
37	GND	NEW	Ground
38	TMPWR	NEW	Termination Power
39	GND	NEW	Ground
40	GND	NEW	Ground
41	/ATN	NEW	Attention
42	n/c	-	Not connected
43	/BSY	NEW	Busy
44	/ACK	NEW	Acknowledge
45	/RST	NEW	Reset
46	/MSG	NEW	Message
47	/SEL	NEW	Select
48	/C/D	NEW	Control/Data
49	/REQ	NEW	Request
50	/I/O	NEW	Input/Output

Note: Direction is Device relative Bus (other Devices).

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

SCSI External (Future Domain) Connector

NEW
NEW
NEW

SCSI External (Future Domain)

NEW (At the controller)

NEW (At the cable)
25 PIN D-SUB FEMALE at the controller.
25 PIN D-SUB MALE at the cable.

Pin	Name	Dir	Description
1	GND	NEW	Ground
2	DB1	NEW	Data Bus 1
3	DB3	NEW	Data Bus 3
4	DB5	NEW	Data Bus 5
5	DB7	NEW	Data Bus 7
6	GND	NEW	Ground
7	/SEL	NEW	Select
8	GND	NEW	Ground
9	TMPWR	NEW	Termination Power
10	/RST	NEW	Reset
11	C/D	NEW	Control/Data
12	I/O	NEW	Input/Output
13	GND	NEW	Ground
14	DB0	NEW	Data Bus 0
15	DB2	NEW	Data Bus 2
16	DB4	NEW	Data Bus 4
17	DB6	NEW	Data Bus 6
18	PARITY	NEW	Data Parity
19	GND	NEW	Ground
20	/ATN	NEW	Attention
21	/MSG	NEW	Message
22	/ACK	NEW	Acknowledge
23	BSY	NEW	Busy
24	/REQ	NEW	Request
25	GND	NEW	Ground

Note: Direction is Device relative Bus (other Devices).

Contributor: Joakim Ogren

Source: TheRef TechTalk

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://theref.c3d.rl.af.mil
Open this address in your WWW browser.

SCSI External (Amiga/Mac) Connector

NEW
NEW
NEW

SCSI External (Amiga/Mac)

NEW (At the controller)

NEW (At the cable)
25 PIN D-SUB FEMALE at the controller.
25 PIN D-SUB MALE at the cable.

Pin	Name	Dir	Description
1	/REQ	NEW	Request
2	/MSG	NEW	Message
3	I/O	NEW	Input/Output
4	/RST	NEW	Reset
5	/ACK	NEW	Acknowledge
6	BSY	NEW	Busy
7	GND	NEW	Ground
8	DB0	NEW	Data Bus 0
9	GND	NEW	Ground
10	DB3	NEW	Data Bus 3
11	DB5	NEW	Data Bus 5
12	DB6	NEW	Data Bus 6
13	DB7	NEW	Data Bus 7
14	GND	NEW	Ground
15	C/D	NEW	Control/Data
16	GND	NEW	Ground
17	/ATN	NEW	Attention
18	GND	NEW	Ground
19	/SEL	NEW	Select
20	PARITY	NEW	Data Parity
21	DB1	NEW	Data Bus 1
22	DB2	NEW	Data Bus 2
23	DB4	NEW	Data Bus 4
24	GND	NEW	Ground
25	TMPWR	NEW	Termination Power

Note: Direction is Device relative Bus (other Devices).

Contributor: Joakim Ogren

Source:?

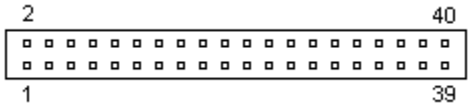
Please send any comments to Joakim Ogren.

IDE Internal Connector

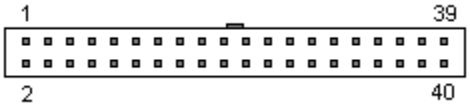
NEW
NEW
NEW

IDE Internal

IDE=Integrated Drive Electronics.
Developed by Compaq and Western Digital.
Newer version of IDE goes under the name ATA=AT bus Attachment.



(At the controller & peripherals)



(At the cable)

40 PIN IDC MALE at the controller & peripherals.
40 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
1	/RESET	NEW	Reset
2	GND	NEW	Ground
3	DD7	NEW	Data 7
4	DD8	NEW	Data 8
5	DD6	NEW	Data 6
6	DD9	NEW	Data 9
7	DD5	NEW	Data 5
8	DD10	NEW	Data 10
9	DD4	NEW	Data 4
10	DD11	NEW	Data 11
11	DD3	NEW	Data 3
12	DD12	NEW	Data 12
13	DD2	NEW	Data 2
14	DD13	NEW	Data 13
15	DD1	NEW	Data 1
16	DD14	NEW	Data 14
17	DD0	NEW	Data 0
18	DD15	NEW	Data 15
19	GND	NEW	Ground
20	KEY	-	Key
21	n/c	-	Not connected
22	GND	NEW	Ground
23	/IOW	NEW	Write Strobe
24	GND	NEW	Ground
25	/IOR	NEW	Read Strobe
26	GND	NEW	Ground
27	IO_CH_RDY	NEW	
28	ALE	?	???
29	n/c	-	Not connected
30	GND	NEW	Ground
31	IRQR	NEW	Interrupt Request

32	/IOCS16	?	IO ChipSelect 16
33	DA1	NEW	Address 1
34	n/c	-	Not connected
35	DA0	NEW	Address 0
36	DA2	NEW	Address 2
37	/IDE_CS0	NEW	(1F0-1F7)
38	/IDE_CS1	NEW	(3F6-3F7)
39	/ACTIVE	NEW	Led driver
40	GND	NEW	Ground

Note: Direction is Controller relative Devices (Harddisks).

Contributor: Joakim Ogren

Source:?

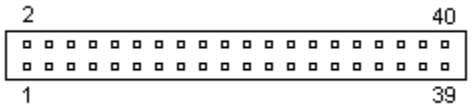
Please send any comments to Joakim Ogren.

ATA Internal Connector

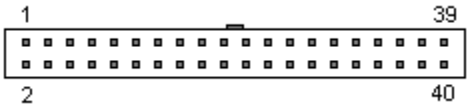
NEW
NEW
NEW

ATA Internal

ATA=AT bus Attachment..
Developed by Western Digital, Conner & Seagate ?.



(At the controller & peripherals)



(At the cable)

40 PIN IDC MALE at the controller & peripherals.
40 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
1	/RESET	NEW	Reset
2	GND	NEW	Ground
3	DD7	NEW	Data 7
4	DD8	NEW	Data 8
5	DD6	NEW	Data 6
6	DD9	NEW	Data 9
7	DD5	NEW	Data 5
8	DD10	NEW	Data 10
9	DD4	NEW	Data 4
10	DD11	NEW	Data 11
11	DD3	NEW	Data 3
12	DD12	NEW	Data 12
13	DD2	NEW	Data 2
14	DD13	NEW	Data 13
15	DD1	NEW	Data 1
16	DD14	NEW	Data 14
17	DD0	NEW	Data 0
18	DD15	NEW	Data 15
19	GND	NEW	Ground
20	KEY	-	Key (Pin missing)
21	DMARQ	?	DMA Request
22	GND	NEW	Ground
23	/DIOW	NEW	Write Strobe
24	GND	NEW	Ground
25	/DIOR	NEW	Read Strobe
26	GND	NEW	Ground
27	IORDY	NEW	I/O Ready
28	SPSYNC:CSEL	?	Spindle Sync or Cable Select
29	/DMACK	?	DMA Acknowledge
30	GND	NEW	Ground
31	INTRQ	NEW	Interrupt Request
32	/IOCS16	?	IO ChipSelect 16

33	DA1	NEW	Address 1
34	PDIAG	?	Passed Diagnositcs
35	DA0	NEW	Address 0
36	DA2	NEW	Address 2
37	/IDE_CS0	NEW	(1F0-1F7)
38	/IDE_CS1	NEW	(3F6-3F7)
39	/ACTIVE	NEW	Led driver
40	GND	NEW	Ground

Note: Direction is Controller relative Devices (Harddisks).

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

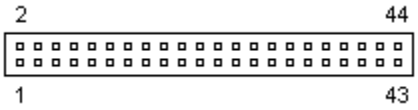
ATA (44) Internal Connector

NEW
NEW
NEW

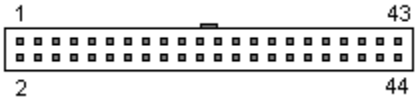
ATA (44) Internal

ATA=AT bus Attachment.

This connector is mostly used for 2.5" internal harddisks.
See ATA for pin 1-40.



(At the controller & peripherals)



(At the cable)

44 PIN IDC (0.75") MALE at the controller & peripherals.
44 PIN IDC (0.75") FEMALE at the cable.

Pin	Name	Dir	Description
41	+5VL	NEW	+5 VDC (Logic)
42	+5VM	NEW	+5 VDC (Motor)
43	GND	NEW	Ground
44	/TYPE	NEW	Type (0=ATA)

Note: Direction is Controller relative Devices (harddisks).

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

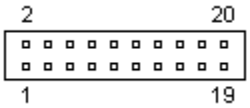
ESDI Connector

NEW
NEW
NEW

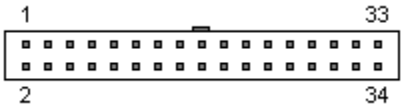
ESDI

ESDI=Enhanced Small Device Interface.
Developed by Maxtor in the early 1980's as an upgrade and improvement to the ST506 design.

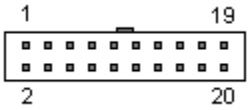
NEW (At the controller)



(At the controller)



(At the harddisk)



(At the harddisk)

34 PIN IDC MALE at the Controller.
20 PIN IDC MALE at the Controller.
34 PIN IDC FEMALE at the Harddisk.
20 PIN IDC FEMALE at the Harddisk.

Control connector

Pin	Name	Description
2		Head Sel 3
4		Head Sel 2
6		Write Gate
8		Config/Stat Data
10		Transfer Acknowledge
12		Attention
14		Head Sel 0
16		Sect/Add MK Found
18		Head Sel 1
20		Index
22		Ready
24		Transfer Request
26		Drive Sel 1
28		Drive Sel 2
30		Drive Sel 3
32		Read Gate
34		Command Data

Note: All odd are GND, Ground.

Data connector

Pin	Name	Description
1		Drive Selected
2		Sect/Add MK Found
3		Seek Complete
4		Address Mark Enable
5		(reserved, for step mode)
6	GND	Ground
7		Write Clock+
8		Write Clock-
9		Cartridge Changed
10		Read Ref Clock+
11		Read Ref Clock-
12	GND	Ground
13		NRZ Write Data+
14		NRZ Write Data-
15	GND	Ground
16	GND	Ground
17		NRZ Read Data+
18		NRZ Read Data-
19	GND	Ground
20	GND	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

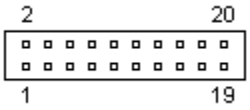
ST506/412 Connector

NEW
NEW
NEW

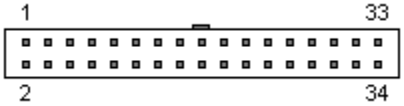
ST506/412

Developed by Seagate.
Also known as MFM or RLL since these are the encoding methods used to store data. Seagate originally developed it to support their ST506 (5 MB) and ST412 (10 MB) drives.
The first drives used an encoding method called MFM (Modified Frequency Modulation). Later a new encoding method was developed, RLL (Run Length Limited). RLL had the advantage that it was possible to store 50% more with it. But it required better drives. This is almost never an problem. Often called 2,7 RLL because the recording scheme involves patterns with no more than 7 successive zeros and no less than two.

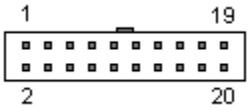
NEW (At the controller)



(At the controller)



(At the harddisk)



(At the harddisk)

34 PIN IDC MALE at the Controller.
20 PIN IDC MALE at the Controller.
34 PIN IDC FEMALE at the Harddisk.
20 PIN IDC FEMALE at the Harddisk.

Control connector

Pin	Name	Description
2		Head Sel 8
4		Head Sel 4
6		Write Gate
8		Seek Complete
10		Track 0
12		Write Fault
14		Head Sel 1
16	RES	(reserved)
18		Head Sel 2
20		Index
22		Ready
24		Step

26	Drive Sel 1
28	Drive Sel 2
30	Drive Sel 3
32	Drive Sel 4
34	Direction In

Note: All odd pins are GND, Ground.

Data connector

Pin	Name	Description
1		Drive Selected
2	GND	Ground
3	RES	(reserved)
4	GND	Ground
5	RES	(reserved)
6	GND	Ground
7	RES	(reserved)
8	GND	Ground
9	RES	(reserved)
10	RES	(reserved)
11	GND	Ground
12	GND	Ground
13		Write Data+
14		Write Data-
15	GND	Ground
16	GND	Ground
17		Read Data+
18		Read Data-
19	GND	Ground
20	GND	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Paravision SX-1 External IDE Connector

NEW
NEW
NEW

Paravision SX-1 External IDE

Paravision was formerly Microbotics.

NEW (At the controller)

37 PIN D-SUB FEMALE at the controller.

Pin	Name	Description
1	/IDE-RESET	Drive Reset
2	D0	Data bit 0
3	D2	Data bit 2
4	D4	Data bit 4
5	D6	Data bit 6
6	GND	Ground
7	D8	Data bit 8
8	D10	Data bit 10
9	D12	Data bit 12
10	D14	Data bit 14
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	+5V	5V Power
19	+5V	5V Power
20	GND	Ground
21	D1	Data bit 1
22	D3	Data bit 3
23	D5	Data bit 5
24	D7	Data bit 7
25	GND	Ground
26	D9	Data bit 9
27	D11	Data bit 11
28	D13	Data bit 13
29	D15	Data bit 15
30	/IOW	I/O Write
31	/IOR	I/O Read
32	IDE-IRQ	Interrupt Request
33	IDE-A2	Address bit 2
34	IDE-A1	Address bit 1
35	IDE-A0	Address bit 0
36	/BICS1	Chip Select 1
37	/BICS0	Chip Select 0

Contributor: Joakim Ogren

Source:SX-1 External IDE connector, usenet posting by Mike Pinso at Paravision.

Please send any comments to Joakim Ogren.

This the e-mail address:
microbotics1@bix.com
Choose this address in your e-mail reader.

C64 Cassette Connector

NEW
NEW
NEW

C64 Cassette

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Dir	Description
A-1	GND	NEW	Ground
B-2	+5V	NEW	+5 Volts DC
C-3	MOTOR	NEW	Cassette Motor
D-4	READ	NEW	Cassette Read
E-5	WRITE	NEW	Cassette Write
F-6	SENSE	?	Cassette Sense

Note: Direction is Computer relative Cassette.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

CoCo Cassette Connector

NEW
NEW
NEW

CoCo Cassette

Availble on the Tandy/Radio Shack Color Computer (CoCo).

NEW (At the CoCo)
UNKNOWN CONNECTOR at the CoCo.

Pin	Description
1	Motor Relay
2	Ground
3	Motor Relay
4	Signal Iinput
5	Signal Ouput

Contributor: Joakim Ogren

Source:Tandy Color Computer FAQ at Video Game Advantage's homepage

Please send any comments to Joakim Ogren.

MSX Cassette Connector

NEW
NEW
NEW

MSX Cassette

NEW (At the computer)

NEW (At the cassette cable)

8 PIN DIN (DIN45326) FEMALE at the computer.

8 PIN DIN (DIN45326) MALE at the cassette cable.

Pin	Name	Dir	Description
1	GND	NEW	Ground
2	GND	NEW	Ground
3	GND	NEW	Ground
4	CMTOUT	NEW	Sount Output
5	CMTIN	NEW	Sound Input
6	REM+	NEW	Remote control (from relay)
7	REM-	NEW	Remote control (from relay)
8	GND	NEW	Ground

Note: Direction is Computer relative Cassette.

Contributor: Joakim Ogren

Source:Mayer's SV738 X'press I/O map

Please send any comments to Joakim Ogren.

30 pin SIMM Connector

NEW
NEW
NEW

30 pin SIMM

SIMM=Single Inline Memory Module.

NEW (At the computer)

30 PIN SIMM at the computer.

Pin	Name	Description
1	VCC	+5 VDC
2	/CAS	Column Address Strobe
3	DQ0	Data 0
4	A0	Address 0
5	A1	Address 1
6	DQ1	Data 1
7	A2	Address 2
8	A3	Address 3
9	GND	Ground
10	DQ2	Data 2
11	A4	Address 4
12	A5	Address 5
13	DQ3	Data 3
14	A6	Address 6
15	A7	Address 7
16	DQ4	Data 4
17	A8	Address 8
18	A9	Address 9
19	A10	Address 10
20	DQ5	Data 5
21	/WE	Write Enable
22	GND	Ground
23	DQ6	Data 6
24	n/c	Not connected
25	DQ7	Data 7
26	QP	Data Parity Out
27	/RAS	Row Address Strobe
28	/CASP	Something Parity ????
29	DP	Data Parity In
30	VCC	+5 VDC

Note: SIMM above is a 4MBx9.
QP & DP is N/C on SIMMs without parity.
A9 is N/C on 256kB.
A10 is N/C on 256kB & 1MB.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

72 pin SIMM Connector

NEW
NEW
NEW

72 pin SIMM

SIMM=Single Inline Memory Module

NEW (At the computer)

72 PIN SIMM at the computer.

Pin	Non-Parity	Parity	Description
1	VSS	VSS	Ground
2	DQ0	DQ0	Data 0
3	DQ18	DQ18	Data 18
4	DQ1	DQ1	Data 1
5	DQ19	DQ19	Data 19
6	DQ2	DQ2	Data 2
7	DQ20	DQ20	Data 20
8	DQ3	DQ3	Data 3
9	DQ21	DQ21	Data 21
10	VCC	VCC	+5 VDC
11	n/c	n/c	Not connected
12	A0	A0	Address 0
13	A1	A1	Address 1
14	A2	A2	Address 2
15	A3	A3	Address 3
16	A4	A4	Address 4
17	A5	A5	Address 5
18	A6	A6	Address 6
19	A10	A10	Address 10
20	DQ4	DQ4	Data 4
21	DQ22	DQ22	Data 22
22	DQ5	DQ5	Data 5
23	DQ23	DQ23	Data 23
24	DQ6	DQ6	Data 6
25	DQ24	DQ24	Data 24
26	DQ7	DQ7	Data 7
27	DQ25	DQ25	Data 25
28	A7	A7	Address 7
29	A11	A11	Address 11
30	VCC	VCC	+5 VDC
31	A8	A8	Address 8
32	A9	A9	Address 9
33	/RAS3	/RAS3	Row Address Strobe 3
34	/RAS2	/RAS2	Row Address Strobe 2
35	n/c	PQ26	Parity 26 (3rd)
36	n/c	PQ8	Parity 8 (1st)
37	n/c	PQ17	Parity 26 (3rd)
38	n/c	PQ35	Parity 35 (4th)
39	VSS	VSS	Ground
40	/CAS0	/CAS0	Column Address Strobe 0
41	/CAS2	/CAS2	Column Address Strobe 2
42	/CAS3	/CAS3	Column Address Strobe 3
43	/CAS1	/CAS1	Column Address Strobe 1
44	/RAS0	/RAS0	Row Address Strobe 0

45	/RAS1	/RAS1	Row Address Strobe 1
46	n/c	n/c	Not connected
47	/WE	/WE	Read/Write
48	n/c	n/c	Not connected
49	DQ9	DQ9	Data 9
50	DQ27	DQ27	Data 27
51	DQ10	DQ10	Data 10
52	DQ28	DQ28	Data 28
53	DQ11	DQ11	Data 11
54	DQ29	DQ29	Data 29
55	DQ12	DQ12	Data 12
56	DQ30	DQ30	Data 30
57	DQ13	DQ13	Data 13
58	DQ31	DQ31	Data 31
59	VCC	VCC	+5 VDC
60	DQ32	DQ32	Data 32
61	DQ14	DQ14	Data 14
62	DQ33	DQ33	Data 33
63	DQ15	DQ15	Data 15
64	DQ34	DQ34	Data 34
65	DQ16	DQ16	Data 16
66	n/c	n/c	Not connected
67	PD1	PD1	Presence Detect 1
68	PD2	PD2	Presence Detect 2
69	PD3	PD3	Presence Detect 3
70	PD4	PD4	Presence Detect 4
71	n/c	n/c	Not connected
72	VSS	VSS	Ground

Notes: A9 is a N/C on 256k and 512k modules.
A10 is a N/C on 256k, 512k, 1M and 4M modules.
RAS1/RAS3 are N/C on 256k, 1M and 4M modules.

Contributor: Joakim Ogren, Mark Brown

Source:Various productsheets at IBM Memory Products

Please send any comments to Joakim Ogren.

This the e-mail address:
bugman@total.net
Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.chips.ibm.com/products/memory/
Open this address in your WWW browser.

72 pin ECC SIMM Connector

NEW
NEW
NEW

72 pin ECC SIMM

SIMM=Single Inline Memory Module
ECC=Error Correcting Code.

NEW (At the computer)
72 PIN SIMM at the computer.

Pin	ECC	Optimized	Description
1	VSS	VSS	Ground
2	DQ0	DQ0	Data 0
3	DQ1	DQ1	Data 1
4	DQ2	DQ2	Data 2
5	DQ3	DQ3	Data 3
6	DQ4	DQ4	Data 4
7	DQ5	DQ5	Data 5
8	DQ6	DQ6	Data 6
9	DQ7	DQ7	Data 7
10	VCC	VCC	+5 VDC
11	PD5	PD5	Presence Detect 5
12	A0	A0	Address 0
13	A1	A1	Address 1
14	A2	A2	Address 2
15	A3	A3	Address 3
16	A4	A4	Address 4
17	A5	A5	Address 5
18	A6	A6	Address 6
19	n/c	n/c	Not connected
20	DQ8	DQ8	Data 8
21	DQ9	DQ9	Data 9
22	DQ10	DQ10	Data 10
23	DQ11	DQ11	Data 11
24	DQ12	DQ12	Data 12
25	DQ13	DQ13	Data 13
26	DQ14	DQ14	Data 14
27	DQ15	DQ15	Data 15
28	A7	A7	Address 7
29	DQ16	DQ16	Data 16
30	VCC	VCC	+5 VDC
31	A8	A8	Address 8
32	A9	A9	Address 9
33	n/c	n/c	Not connected
34	/RAS1	/RAS1	Row Address Strobe 1
35	DQ17	DQ17	Data 17
36	DQ18	DQ18	Data 18
37	DQ19	DQ19	Data 19
38	DQ20	DQ20	Data 20
39	VSS	VSS	Ground
40	/CAS0	/CAS0	Column Address Strobe 0
41	A10	A10	Address 10
42	A11	A11	Address 11

43	/CAS1	/CAS1	Column Address Strobe 1
44	/RAS0	/RAS0	Row Address Strobe 0
45	/RAS1	/RAS1	Row Address Strobe 1
46	DQ21	DQ21	Data 21
47	/WE	/WE	Read/Write
48	/ECC	/ECC	
49	DQ22	DQ22	Data 22
50	DQ23	DQ23	Data 23
51	DQ24	DQ24	Data 24
52	DQ25	DQ25	Data 25
53	DQ26	DQ26	Data 26
54	DQ27	DQ27	Data 27
55	DQ28	DQ28	Data 28
56	DQ29	DQ29	Data 29
57	DQ30	DQ30	Data 30
58	DQ31	DQ31	Data 31
59	VCC	VCC	+5 VDC
60	DQ32	DQ32	Data 32
61	DQ33	DQ33	Data 33
62	DQ34	DQ34	Data 34
63	DQ35	DQ35	Data 35
64	n/c	DQ36	Data 36
65	n/c	DQ37	Data 37
66	n/c	DQ38	Data 38
67	PD1	PD1	Presence Detect 1
68	PD2	PD2	Presence Detect 2
69	PD3	PD3	Presence Detect 3
70	PD4	PD4	Presence Detect 4
71	n/c	DQ39	Data 39
72	VSS	VSS	Ground

Contributor: Joakim Ogren

Source:Various productsheets at IBM Memory Products

Please send any comments to Joakim Ogren.

72 pin SO DIMM Connector

NEW
NEW
NEW

72 pin SO DIMM

SO DIMM=Small Outline Dual Inline Memory Module

NEW (At the computer)

72 PIN SO DIMM at the computer.

Pin	Non-Parity	Parity	Description
1	VSS	VSS	Ground
2	DQ0	DQ0	Data 0
3	DQ1	DQ1	Data 1
4	DQ2	DQ2	Data 2
5	DQ3	DQ3	Data 3
6	DQ4	DQ4	Data 4
7	DQ5	DQ5	Data 5
8	DQ6	DQ6	Data 6
9	DQ7	DQ7	Data 7
10	VCC	VCC	+5 VDC
11	PD1	PD1	Presence Detect 1
12	A0	A0	Address 0
13	A1	A1	Address 1
14	A2	A2	Address 2
15	A3	A3	Address 3
16	A4	A4	Address 4
17	A5	A5	Address 5
18	A6	A6	Address 6
19	A10	A10	Address 10
20	n/c	PQ8	Data 8 (Parity 1)
21	DQ9	DQ9	Data 9
22	DQ10	DQ10	Data 10
23	DQ11	DQ11	Data 11
24	DQ12	DQ12	Data 12
25	DQ13	DQ13	Data 13
26	DQ14	DQ14	Data 14
27	DQ15	DQ15	Data 15
28	A7	A7	Address 7
29	A11	A11	Address 11
30	VCC	VCC	+5 VDC
31	A8	A8	Address 8
32	A9	A9	Address 9
33	/RAS3	RAS3	Row Address Strobe 3
34	/RAS2	RAS2	Row Address Strobe 2
35	DQ16	DQ16	Data 16
36	n/c	PQ17	Data 17 (Parity 2)
37	DQ18	DQ18	Data 18
38	DQ19	DQ19	Data 19
39	VSS	VSS	Ground
40	/CAS0	CAS0	Column Address Strobe 0
41	/CAS2	CAS2	Column Address Strobe 2
42	/CAS3	CAS3	Column Address Strobe 3
43	/CAS1	CAS1	Column Address Strobe 1
44	/RAS0	RAS0	Row Address Strobe 0

45	/RAS1	RAS1	Row Address Strobe 1
46	A12	A12	Address 12
47	/WE	WE	Read/Write
48	A13	A13	Address 13
49	DQ20	DQ20	Data 20
50	DQ21	DQ21	Data 21
51	DQ22	DQ22	Data 22
52	DQ23	DQ23	Data 23
53	DQ24	DQ24	Data 24
54	DQ25	DQ25	Data 25
55	n/c	PQ26	Data 26
56	DQ27	DQ27	Data 27 (Parity 3)
57	DQ28	DQ28	Data 28
58	DQ29	DQ29	Data 29
59	DQ31	DQ31	Data 31
60	DQ30	DQ30	Data 30
61	VCC	VCC	+5 VDC
62	DQ32	DQ32	Data 32
63	DQ33	DQ33	Data 33
64	DQ34	DQ34	Data 34
65	n/c	PQ35	Data 35 (Parity 4)
66	PD2	PD2	Presence Detect 2
67	PD3	PD3	Presence Detect 3
68	PD4	PD4	Presence Detect 4
69	PD5	PD5	Presence Detect 1
70	PD6	PD6	Presence Detect 6
71	PD7	PD7	Presence Detect 7
72	VSS	VSS	Ground

Contributor: Joakim Ogren, Mark Brown

Source:Various productsheets at IBM Memory Products

Please send any comments to Joakim Ogren.

144 pin SO DIMM Connector

NEW
NEW
NEW

144 pin SO DIMM

SO SIMM=Small Outline Single Inline Memory Module

NEW (At the computer)

144 PIN SO SIMM at the computer.

Pin	Normal	ECC	Description
1	VSS	VSS	Ground
2	VSS	VSS	Ground
3	DQ0	DQ0	Data 0
4	DQ32	DQ32	Data 32
5	DQ1	DQ1	Data 1
6	DQ33	DQ33	Data 33
7	DQ2	DQ2	Data 2
8	DQ34	DQ34	Data 34
9	DQ3	DQ3	Data 3
10	DQ35	DQ35	Data 35
11	VCC	VCC	+5 VDC
12	VCC	VCC	+5 VDC
13	DQ4	DQ4	Data 4
14	DQ36	DQ36	Data 36
15	DQ5	DQ5	Data 5
16	DQ37	DQ37	Data 37
17	DQ6	DQ6	Data 6
18	DQ38	DQ38	Data 38
19	DQ7	DQ7	Data 7
20	DQ39	DQ39	Data 39
21	VSS	VSS	Ground
22	VSS	VSS	Ground
23	/CAS0	/CAS0	Column Address Strobe 0
24	/CAS4	/CAS4	Column Address Strobe 4
25	/CAS1	/CAS1	Column Address Strobe 1
26	/CAS5	/CAS5	Column Address Strobe 5
27	VCC	VCC	+5 VDC
28	VCC	VCC	+5 VDC
29	A0	A0	Address 0
30	A3	A3	Address 3
31	A1	A1	Address 1
32	A4	A4	Address 4
33	A2	A2	Address 2
34	A5	A5	Address 5
35	VSS	VSS	Ground
36	VSS	VSS	Ground
37	DQ8	DQ8	Data 8
38	DQ40	DQ40	Data 40
39	DQ9	DQ9	Data 9
40	DQ41	DQ41	Data 41
41	DQ10	DQ10	Data 10
42	DQ42	DQ42	Data 42
43	DQ11	DQ11	Data 11
44	DQ43	DQ43	Data 43

45	VCC	VCC	+5 VDC
46	VCC	VCC	+5 VDC
47	DQ12	DQ12	Data 12
48	DQ44	DQ44	Data 44
49	DQ13	DQ13	Data 13
50	DQ45	DQ45	Data 45
51	DQ14	DQ14	Data 14
52	DQ46	DQ46	Data 46
53	DQ15	DQ15	Data 15
54	DQ47	DQ47	Data 47
55	VSS	VSS	Ground
56	VSS	VSS	Ground
57	n/c	CB0	
58	n/c	CB4	
59	n/c	CB1	
60	n/c	CB5	
61	DU	DU	Don't use
62	DU	DU	Don't use
63	VCC	VCC	+5 VDC
64	VCC	VCC	+5 VDC
65	DU	DU	Don't use
66	DU	DU	Don't use
67	/WE	/WE	Read/Write
68	n/c	n/c	Not connected
69	/RAS0	/RAS0	Row Address Strobe 0
70	n/c	n/c	Not connected
71	/RAS1	/RAS1	Row Address Strobe 1
72	n/c	n/c	Not connected
73	/OE	/OE	
74	n/c	n/c	Not connected
75	VSS	VSS	Ground
76	VSS	VSS	Ground
77	n/c	CB2	
78	n/c	CB6	
79	n/c	CB3	
80	n/c	CB7	
81	VCC	VCC	+5 VDC
82	VCC	VCC	+5 VDC
83	DQ16	DQ16	Data 16
84	DQ48	DQ48	Data 48
85	DQ17	DQ17	Data 17
86	DQ49	DQ49	Data 49
87	DQ18	DQ18	Data 18
88	DQ50	DQ50	Data 50
89	DQ19	DQ19	Data 19
90	DQ51	DQ51	Data 51
91	VSS	VSS	Ground
92	VSS	VSS	Ground
93	DQ20	DQ20	Data 20
94	DQ52	DQ52	Data 52
95	DQ21	DQ21	Data 21
96	DQ53	DQ53	Data 53
97	DQ22	DQ22	Data 22
98	DQ54	DQ54	Data 54
99	DQ23	DQ23	Data 23
100	DQ55	DQ55	Data 55

101	VCC	VCC	+5 VDC
102	VCC	VCC	+5 VDC
103	A6	A6	Adress 6
104	A7	A7	Adress 7
105	A8	A8	Adress 8
106	A11	A11	Adress 11
107	VSS	VSS	Ground
108	VSS	VSS	Ground
109	A9	A9	Adress 9
110	A12	A12	Adress 12
111	A10	A10	Adress 10
112	A13	A13	Adress 13
113	VCC	VCC	+5 VDC
114	VCC	VCC	+5 VDC
115	/CAS2	/CAS2	Column Address Strobe 2
116	/CAS6	/CAS6	Column Address Strobe 6
117	/CAS3	/CAS3	Column Address Strobe 3
118	/CAS7	/CAS7	Column Address Strobe 7
119	VSS	VSS	Ground
120	/VSS	/VSS	Ground
121	DQ24	DQ24	Data 24
122	DQ56	DQ56	Data 56
123	DQ25	DQ25	Data 25
124	DQ57	DQ57	Data 57
125	DQ26	DQ26	Data 26
126	DQ58	DQ58	Data 58
127	DQ27	DQ27	Data 27
128	DQ59	DQ59	Data 59
129	VCC	VCC	+5 VDC
130	VCC	VCC	+5 VDC
131	DQ28	DQ28	Data 28
132	DQ60	DQ60	Data 60
133	DQ29	DQ29	Data 29
134	DQ61	DQ61	Data 61
135	DQ30	DQ30	Data 30
136	DQ62	DQ62	Data 62
137	DQ31	DQ31	Data 31
138	DQ63	DQ63	Data 63
139	VSS	VSS	Ground
140	VSS	VSS	Ground
141	SDA	SDA	
142	SCL	SCL	
143	VCC	VCC	+5 VDC
144	VCC	VCC	+5 VDC

Contributor: Joakim Ogren, Mark Brown

Source:Various productsheets at IBM Memory Products

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

168 pin DRAM DIMM (Unbuffered)

DIMM=Dual Inline Memory Module

NEW (At the computer)
168 PIN DIMM at the computer.
Front Side (left side 1-42, right side 43-84)
Back Side (left side 85-126, right side 127-168)

Front, Left

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description
1	VSS	VSS	VSS	VSS	Ground
2	DQ0	DQ0	DQ0	DQ0	Data 0
3	DQ1	DQ1	DQ1	DQ1	Data 1
4	DQ2	DQ2	DQ2	DQ2	Data 2
5	DQ3	DQ3	DQ3	DQ3	Data 3
6	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
7	DQ4	DQ4	DQ4	DQ4	Data 4
8	DQ5	DQ5	DQ5	DQ5	Data 5
9	DQ6	DQ6	DQ6	DQ6	Data 6
10	DQ7	DQ7	DQ7	DQ7	Data 7
11	DQ8	DQ8	DQ8	DQ8	Data 8
12	VSS	VSS	VSS	VSS	Ground
13	DQ9	DQ9	DQ9	DQ9	Data 9
14	DQ10	DQ10	DQ10	DQ10	Data 10
15	DQ11	DQ11	DQ11	DQ11	Data 11
16	DQ12	DQ12	DQ12	DQ12	Data 12
17	DQ13	DQ13	DQ13	DQ13	Data 13
18	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
19	DQ14	DQ14	DQ14	DQ14	Data 14
20	DQ15	DQ15	DQ15	DQ15	Data 15
21	n/c	CB0	CB0	CB0	Parity/Check Bit Input/Output 0
22	n/c	CB1	CB1	CB1	Parity/Check Bit Input/Output 1
23	VSS	VSS	VSS	VSS	Ground
24	n/c	n/c	n/c	CB8	Parity/Check Bit Input/Output 8
25	n/c	n/c	n/c	CB9	Parity/Check Bit Input/Output 9
26	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
27	/WE0	/WE0	/WE0	/WE0	Read/Write Input
28	/CAS0	/CAS0	/CAS0	/CAS0	Column Address Strobe 0
29	/CAS1	/CAS1	/CAS1	/CAS1	Column Address Strobe 1
30	/RAS0	/RAS0	/RAS0	/RAS0	Row Address Strobe 0
31	/OE0	/OE0	/OE0	/OE0	Output Enable
32	VSS	VSS	VSS	VSS	Ground
33	A0	A0	A0	A0	Address 0
34	A2	A2	A2	A2	Address 2
35	A4	A4	A4	A4	Address 4
36	A6	A6	A6	A6	Address 6
37	A8	A8	A8	A8	Address 8
38	A10	A10	A10	A10	Address 10

39	A12	A12	A12	A12	Address 12
40	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
41	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
42	DU	DU	DU	DU	Don't Use

Front, Right

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description
43	VSS	VSS	VSS	VSS	Ground
44	/OE2	/OE2	/OE2	/OE2	
45	/RAS2	/RAS2	/RAS2	/RAS2	Row Address Strobe 2
46	/CAS2	/CAS2	/CAS2	/CAS2	Column Address Strobe 2
47	/CAS3	/CAS3	/CAS3	/CAS3	Column Address Strobe 3
48	/WE2	/WE2	/WE2	/WE2	Read/Write Input
49	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
50	n/c	n/c	n/c	CB10	Parity/Check Bit Input/Output 10
51	n/c	n/c	n/c	CB11	Parity/Check Bit Input/Output 11
52	n/c	CB2	CB2	CB2	Parity/Check Bit Input/Output 2
53	n/c	CB3	CB3	CB3	Parity/Check Bit Input/Output 3
54	VSS	VSS	VSS	VSS	Ground
55	DQ16	DQ16	DQ16	DQ16	Data 16
56	DQ17	DQ17	DQ17	DQ17	Data 17
57	DQ18	DQ18	DQ18	DQ18	Data 18
58	DQ19	DQ19	DQ19	DQ19	Data 19
59	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
60	DQ20	DQ20	DQ20	DQ20	Data 20
61	n/c	n/c	n/c	n/c	Not connected
62	DU	DU	DU	DU	Don't Use
63	n/c	n/c	n/c	n/c	Not connected
64	VSS	VSS	VSS	VSS	Ground
65	DQ21	DQ21	DQ21	DQ21	Data 21
66	DQ22	DQ22	DQ22	DQ22	Data 22
67	DQ23	DQ23	DQ23	DQ23	Data 23
68	VSS	VSS	VSS	VSS	Ground
69	DQ24	DQ24	DQ24	DQ24	Data 24
70	DQ25	DQ25	DQ25	DQ25	Data 25
71	DQ26	DQ26	DQ26	DQ26	Data 26
72	DQ27	DQ27	DQ27	DQ27	Data 27
73	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
74	DQ28	DQ28	DQ28	DQ28	Data 28
75	DQ29	DQ29	DQ29	DQ29	Data 29
76	DQ30	DQ30	DQ30	DQ30	Data 30
77	DQ31	DQ31	DQ31	DQ31	Data 31
78	VSS	VSS	VSS	VSS	Ground
79	n/c	n/c	n/c	n/c	Not connected
80	n/c	n/c	n/c	n/c	Not connected
81	n/c	n/c	n/c	n/c	Not connected
82	SDA	SDA	SDA	SDA	Serial Data
83	SCL	SCL	SCL	SCL	Serial Clock
84	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC

Back, Left

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description
85	VSS	VSS	VSS	VSS	Ground
86	DQ32	DQ32	DQ32	DQ32	Data 32
87	DQ33	DQ33	DQ33	DQ33	Data 33

88	DQ34	DQ34	DQ34	DQ34	Data 34
89	DQ35	DQ35	DQ35	DQ35	Data 35
90	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
91	DQ36	DQ36	DQ36	DQ36	Data 36
92	DQ37	DQ37	DQ37	DQ37	Data 37
93	DQ38	DQ38	DQ38	DQ38	Data 38
94	DQ39	DQ39	DQ39	DQ39	Data 39
95	DQ40	DQ40	DQ40	DQ40	Data 40
96	VSS	VSS	VSS	VSS	Ground
97	DQ41	DQ41	DQ41	DQ41	Data 41
98	DQ42	DQ42	DQ42	DQ42	Data 42
99	DQ43	DQ43	DQ43	DQ43	Data 43
100	DQ44	DQ44	DQ44	DQ44	Data 44
101	DQ45	DQ45	DQ45	DQ45	Data 45
102	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
103	DQ46	DQ46	DQ46	DQ46	Data 46
104	DQ47	DQ47	DQ47	DQ47	Data 47
105	n/c	CB4	CB4	CB4	Parity/Check Bit Input/Output 4
106	n/c	CB5	CB5	CB5	Parity/Check Bit Input/Output 5
107	VSS	VSS	VSS	VSS	Ground
108	n/c	n/c	n/c	CB12	Parity/Check Bit Input/Output 12
109	n/c	n/c	n/c	CB13	Parity/Check Bit Input/Output 13
110	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
111	DU	DU	DU	DU	Don't Use
112	/CAS4	/CAS4	/CAS4	/CAS4	Column Address Strobe 4
113	/CAS5	/CAS5	/CAS5	/CAS5	Column Address Strobe 5
114	/RAS1	/RAS1	/RAS1	/RAS1	Row Address Strobe 1
115	DU	DU	DU	DU	Don't Use
116	VSS	VSS	VSS	VSS	Ground
117	A1	A1	A1	A1	Address 1
118	A3	A3	A3	A3	Address 3
119	A5	A5	A5	A5	Address 5
120	A7	A7	A7	A7	Address 7
121	A9	A9	A9	A9	Address 9
122	A11	A11	A11	A11	Address 11
123	A13	A13	A13	A13	Address 13
124	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
125	DU	DU	DU	DU	Don't Use
126	DU	DU	DU	DU	Don't Use

Back, Right

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description
127	VSS	VSS	VSS	VSS	Ground
128	DU	DU	DU	DU	Don't Use
129	/RAS3	/RAS3	/RAS3	/RAS3	Column Address Strobe 3
130	/CAS6	/CAS6	/CAS6	/CAS6	Column Address Strobe 6
131	/CAS7	/CAS7	/CAS7	/CAS7	Column Address Strobe 7
132	DU	DU	DU	DU	Don't Use
133	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
134	n/c	n/c	n/c	CB14	Parity/Check Bit Input/Output 14
135	n/c	n/c	n/c	CB15	Parity/Check Bit Input/Output 15
136	n/c	CB6	CB6	CB6	Parity/Check Bit Input/Output 6
137	n/c	CB7	CB7	CB7	Parity/Check Bit Input/Output 7
138	VSS	VSS	VSS	VSS	Ground
139	DQ48	DQ48	DQ48	DQ48	Data 48

140	DQ49	DQ49	DQ49	DQ49	Data 49
141	DQ50	DQ50	DQ50	DQ50	Data 50
142	DQ51	DQ51	DQ51	DQ51	Data 51
143	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
144	DQ52	DQ52	DQ52	DQ52	Data 52
145	n/c	n/c	n/c	n/c	Not connected
146	DU	DU	DU	DU	Don't Use
147	n/c	n/c	n/c	n/c	Not connected
148	VSS	VSS	VSS	VSS	Ground
149	DQ53	DQ53	DQ53	DQ53	Data 53
150	DQ54	DQ54	DQ54	DQ54	Data 54
151	DQ55	DQ55	DQ55	DQ55	Data 55
152	VSS	VSS	VSS	VSS	Ground
153	DQ56	DQ56	DQ56	DQ56	Data 56
154	DQ57	DQ57	DQ57	DQ57	Data 57
155	DQ58	DQ58	DQ58	DQ58	Data 58
156	DQ59	DQ59	DQ59	DQ59	Data 59
157	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
158	DQ60	DQ60	DQ60	DQ60	Data 60
159	DQ61	DQ61	DQ61	DQ61	Data 61
160	DQ62	DQ62	DQ62	DQ62	Data 62
161	DQ63	DQ63	DQ63	DQ63	Data 63
162	VSS	VSS	VSS	VSS	Ground
163	CK3	CK3	CK3	CK3	
164	n/c	n/c	n/c	n/c	Not connected
165	SA0	SA0	SA0	SA0	Serial Address 0
166	SA1	SA1	SA1	SA1	Serial Address 1
167	SA2	SA2	SA2	SA2	Serial Address 2
168	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC

Contributor: Joakim Ogren, Mark Brown

Source:Various productsheets at IBM Memory Products

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

168 pin SDRAM DIMM (Unbuffered)

DIMM=Dual Inline Memory Module

NEW (At the computer)
168 PIN DIMM at the computer.
Front Side (left side 1-42, right side 43-84)
Back Side (left side 85-126, right side 127-168)

Front, Left

Pin	Non-Parity	72 ECC?	80 ECC?	Description
1	VSS	VSS	VSS	Ground
2	DQ0	DQ0	DQ0	Data 0
3	DQ1	DQ1	DQ1	Data 1
4	DQ2	DQ2	DQ2	Data 2
5	DQ3	DQ3	DQ3	Data 3
6	VDD	VDD	VDD	+5 VDC or +3.3 VDC
7	DQ4	DQ4	DQ4	Data 4
8	DQ5	DQ5	DQ5	Data 5
9	DQ6	DQ6	DQ6	Data 6
10	DQ7	DQ7	DQ7	Data 7
11	DQ8	DQ8	DQ8	Data 8
12	VSS	VSS	VSS	Ground
13	DQ9	DQ9	DQ9	Data 9
14	DQ10	DQ10	DQ10	Data 10
15	DQ11	DQ11	DQ11	Data 11
16	DQ12	DQ12	DQ12	Data 12
17	DQ13	DQ13	DQ13	Data 13
18	VDD	VDD	VDD	+5 VDC or +3.3 VDC
19	DQ14	DQ14	DQ14	Data 14
20	DQ15	DQ15	DQ15	Data 15
21	n/c	CB0	CB0	Parity/Check Bit Input/Output 0
22	n/c	CB1	CB1	Parity/Check Bit Input/Output 01
23	VSS	VSS	VSS	Ground
24	n/c	n/c	CB8	Parity/Check Bit Input/Output 8
25	n/c	n/c	CB9	Parity/Check Bit Input/Output 9
26	VDD	VDD	VDD	+5 VDC or +3.3 VDC
27	/WE	/WE	/WE	Read/Write
28	DQMB0	DQMB0	DQMB0	Byte Mask signal 0
29	DQMB1	DQMB1	DQMB1	Byte Mask signal 1
30	/S0	/S0	/S0	Chip Select 0
31	DU	DU	DU	Don't Use
32	VSS	VSS	VSS	Ground
33	A0	A0	A0	Address 0
34	A2	A2	A2	Address 2
35	A4	A4	A4	Address 4
36	A6	A6	A6	Address 6
37	A8	A8	A8	Address 8
38	A10/AP	A10/AP	A10/AP	Address 10

39	BA1	BA1	BA1	Bank Address 1
40	VDD	VDD	VDD	+5 VDC or +3.3 VDC
41	VDD	VDD	VDD	+5 VDC or +3.3 VDC
42	CK0	CK0	CK0	Clock signal 0

Front, Right

Pin	Non-Parity	72 ECC?	80 ECC?	Description
43	VSS	VSS	VSS	Ground
44	DU	DU	DU	Don't Use
45	/S2	/S2	/S2	Chip Select 2
46	DQMB2	DQMB2	DQMB2	Byte Mask signal 2
47	DQMB3	DQMB3	DQMB3	Byte Mask signal 3
48	DU	DU	DU	Don't Use
49	VDD	VDD	VDD	+5 VDC or +3.3 VDC
50	n/c	n/c	CB10	Parity/Check Bit Input/Output 10
51	n/c	n/c	CB11	Parity/Check Bit Input/Output 11
52	n/c	CB2	CB2	Parity/Check Bit Input/Output 2
53	n/c	CB3	CB3	Parity/Check Bit Input/Output 3
54	VSS	VSS	VSS	Ground
55	DQ16	DQ16	DQ16	Data 16
56	DQ17	DQ17	DQ17	Data 17
57	DQ18	DQ18	DQ18	Data 18
58	DQ19	DQ19	DQ19	Data 19
59	VDD	VDD	VDD	+5 VDC or +3.3 VDC
60	DQ20	DQ20	DQ20	Data 20
61	n/c	n/c	n/c	Not connected
62	Vref,NC	Vref,NC	Vref,NC	
63	CKE1	CKE1	CKE1	Clock Enable Signal 1
64	VSS	VSS	VSS	Ground
65	DQ21	DQ21	DQ21	Data 21
66	DQ22	DQ22	DQ22	Data 22
67	DQ23	DQ23	DQ23	Data 23
68	VSS	VSS	VSS	Ground
69	DQ24	DQ24	DQ24	Data 24
70	DQ25	DQ25	DQ25	Data 25
71	DQ26	DQ26	DQ26	Data 26
72	DQ27	DQ27	DQ27	Data 27
73	VDD	VDD	VDD	+5 VDC or +3.3 VDC
74	DQ28	DQ28	DQ28	Data 28
75	DQ29	DQ29	DQ29	Data 29
76	DQ30	DQ30	DQ30	Data 30
77	DQ31	DQ31	DQ31	Data 31
78	VSS	VSS	VSS	Ground
79	CK2	CK2	CK2	Clock signal 2
80	n/c	n/c	n/c	Not connected
81	n/c	n/c	n/c	Not connected
82	SDA	SDA	SDA	Serial Data
83	SCL	SCL	SCL	Serial Clock
84	VDD	VDD	VDD	+5 VDC or +3.3 VDC

Back, Left

Pin	Non-Parity	72 ECC?	80 ECC?	Description
85	VSS	VSS	VSS	Ground
86	DQ32	DQ32	DQ32	Data 32
87	DQ33	DQ33	DQ33	Data 33

88	DQ34	DQ34	DQ34	Data 34
89	DQ35	DQ35	DQ35	Data 35
90	VDD	VDD	VDD	+5 VDC or +3.3 VDC
91	DQ36	DQ36	DQ36	Data 36
92	DQ37	DQ37	DQ37	Data 37
93	DQ38	DQ38	DQ38	Data 38
94	DQ39	DQ39	DQ39	Data 39
95	DQ40	DQ40	DQ40	Data 40
96	VSS	VSS	VSS	Ground
97	DQ41	DQ41	DQ41	Data 41
98	DQ42	DQ42	DQ42	Data 42
99	DQ43	DQ43	DQ43	Data 43
100	DQ44	DQ44	DQ44	Data 44
101	DQ45	DQ45	DQ45	Data 45
102	VDD	VDD	VDD	+5 VDC or +3.3 VDC
103	DQ46	DQ46	DQ46	Data 46
104	DQ47	DQ47	DQ47	Data 47
105	n/c	CB4	CB4	Parity/Check Bit Input/Output 4
106	n/c	CB5	CB5	Parity/Check Bit Input/Output 5
107	VSS	VSS	VSS	Ground
108	n/c	n/c	CB12	Parity/Check Bit Input/Output 12
109	n/c	n/c	CB13	Parity/Check Bit Input/Output 13
110	VDD	VDD	VDD	+5 VDC or +3.3 VDC
111	/CAS	/CAS	/CAS	Column Address Strobe
112	DQMB4	DQMB4	DQMB4	Byte Mask signal 4
113	DQMB5	DQMB5	DQMB5	Byte Mask signal 5
114	/S1	/S1	/S1	Chip Select 1
115	/RAS	/RAS	/RAS	Row Address Strobe
116	VSS	VSS	VSS	Ground
117	A1	A1	A1	Address 1
118	A3	A3	A3	Address 3
119	A5	A5	A5	Address 5
120	A7	A7	A7	Address 7
121	A9	A9	A9	Address 9
122	BA0	BA0	BA0	Bank Address 0
123	A11	A11	A11	Address 11
124	VDD	VDD	VDD	+5 VDC or +3.3 VDC
125	CK1	CK1	CK1	Clock signal 1
126	A12	A12	A12	Address 12

Back, Right

Pin	Non-Parity	72 ECC?	80 ECC?	Description
127	VSS	VSS	VSS	Ground
128	CKE0	CKE0	CKE0	Clock Enable Signal 0
129	/S3	/S3	/S3	Chip Select 3
130	DQMB6	DQMB6	DQMB6	Byte Mask signal 6
131	DQMB7	DQMB7	DQMB7	Byte Mask signal 7
132	A13	A13	A13	Address 13
133	VDD	VDD	VDD	+5 VDC or +3.3 VDC
134	n/c	n/c	CB14	Parity/Check Bit Input/Output 14
135	n/c	n/c	CB15	Parity/Check Bit Input/Output 15
136	n/c	CB6	CB6	Parity/Check Bit Input/Output 6
137	n/c	CB7	CB7	Parity/Check Bit Input/Output 7
138	VSS	VSS	VSS	Ground
139	DQ48	DQ48	DQ48	Data 48

140	DQ49	DQ49	DQ49	Data 49
141	DQ50	DQ50	DQ50	Data 50
142	DQ51	DQ51	DQ51	Data 51
143	VDD	VDD	VDD	+5 VDC or +3.3 VDC
144	DQ52	DQ52	DQ52	Data 52
145	n/c	n/c	n/c	Not connected
146	Vref,NC	Vref,NC	Vref,NC	
147	n/c	n/c	n/c	Not connected
148	VSS	VSS	VSS	Ground
149	DQ53	DQ53	DQ53	Data 53
150	DQ54	DQ54	DQ54	Data 54
151	DQ55	DQ55	DQ55	Data 55
152	VSS	VSS	VSS	Ground
153	DQ56	DQ56	DQ56	Data 56
154	DQ57	DQ57	DQ57	Data 57
155	DQ58	DQ58	DQ58	Data 58
156	DQ59	DQ59	DQ59	Data 59
157	VDD	VDD	VDD	+5 VDC or +3.3 VDC
158	DQ60	DQ60	DQ60	Data 60
159	DQ61	DQ61	DQ61	Data 61
160	DQ62	DQ62	DQ62	Data 62
161	DQ63	DQ63	DQ63	Data 63
162	VSS	VSS	VSS	Ground
163	CK3	CK3	CK3	Clock signal 3
164	n/c	n/c	n/c	Not connected
165	SA0	SA0	SA0	Serial address 0
166	SA1	SA1	SA1	Serial address 1
167	SA2	SA2	SA2	Serial address 2
168	VDD	VDD	VDD	+5 VDC or +3.3 VDC

Contributor: Joakim Ogren

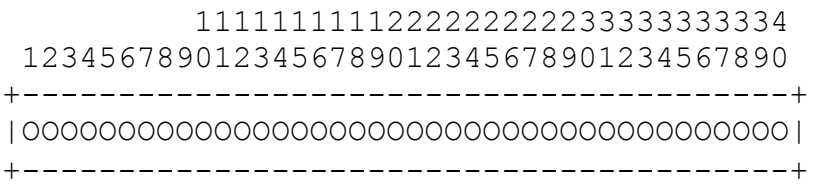
Source:Various productsheets at IBM Memory Products

Please send any comments to Joakim Ogren.

CDTV Memory Card Connector

NEW
NEW
NEW

CDTV Memory Card Port



NEW (At the computer)
40 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	D0	Data Bus 0
2	D1	Data Bus 1
3	D2	Data Bus 2
4	D3	Data Bus 3
5	D4	Data Bus 4
6	D5	Data Bus 5
7	D6	Data Bus 6
8	D7	Data Bus 7
9	D8	Data Bus 8
10	D9	Data Bus 9
11	D10	Data Bus 10
12	D11	Data Bus 11
13	D12	Data Bus 12
14	D13	Data Bus 13
15	D14	Data Bus 14
16	D15	Data Bus 15
17	A1	Address Bus 1
18	A2	Address Bus 2
19	A3	Address Bus 3
20	A4	Address Bus 4
21	A5	Address Bus 5
22	A6	Address Bus 6
23	A7	Address Bus 7
24	A8	Address Bus 8
25	A9	Address Bus 9
26	A10	Address Bus 10
27	A11	Address Bus 11
28	A12	Address Bus 12
29	A13	Address Bus 13
30	A14	Address Bus 14
31	A15	Address Bus 15
32	A16	Address Bus 16
33	A17	Address Bus 17
34	R/W	Read/Write (High=Read)
35	/CSMCOD	Chip Select Odd Bytes
36	/CSMCEN	Chip Select Even Bytes
37	VCC	+5 Volts DC
38	GND	Ground
39	A18	Address Bus 18 (Short J16 to connect A18 to processor bus)

40 A19 Address Bus 19 (Short J17 to connect A19 to processor bus)

Note: Address space=$E00000-$E7FFFF

Contributor: Joakim Ogren

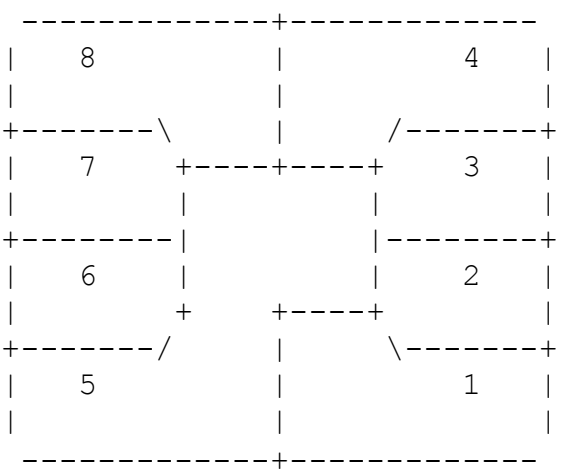
Source:Darren Ewaniuk's CDTV Technical Information

Please send any comments to Joakim Ogren.

SmartCard AFNOR Connector

NEW
NEW
NEW

SmartCard AFNOR



NEW (At the card)

UNKNOWN CONNECTOR at the card.

Pin	Name	Description
1	VCC	+5 VDC
2	R/W	Read/Write
3	CLOCK	Clock
4	RESET	Reset
5	GND	Ground
6	VPP	+21 VDC
7	I/O	In/Out
8	FUSE	Fuse

Contributor: Joakim Ogren

Source: Telecard/Smartcard Technical Spec & Info by Stephane Bausson

Please send any comments to Joakim Ogren.

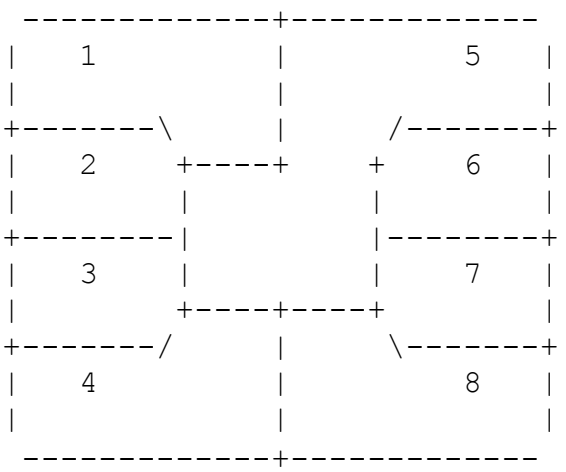
This is the URL for the WWW page:
http://www.physic.ut.ee/~kalev/smartcar.txt
Open this address in your WWW browser.

This the e-mail address:
sbausson@ensem.u-nancy.fr
Choose this address in your e-mail reader.

SmartCard ISO 7816-2 Connector

NEW
NEW
NEW

SmartCard ISO 7816-2



NEW (At the card)

UNKNOWN CONNECTOR at the card.

Pin	Name	Description
1	VCC	+5 VDC
2	RESET	Reset
3	CLOCK	Clock
4	n/c	Not connected
5	GND	Ground
6	n/c	Not connected
7	I/O	In/Out
8	n/c	Not connected

Contributor: Joakim Ogren

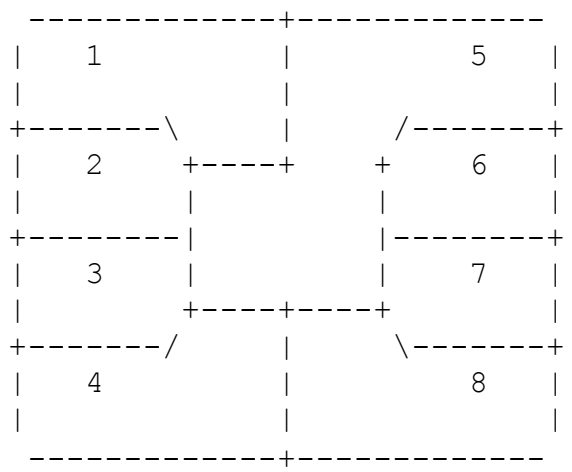
Source:Telecard/Smartcard Technical Spec & Info by Stephane Bausson

Please send any comments to Joakim Ogren.

SmartCard ISO Connector

NEW
NEW
NEW

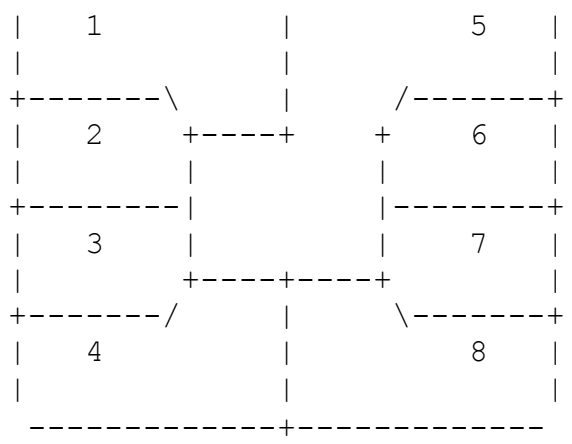
SmartCard ISO



NEW (At the card)
UNKNOWN CONNECTOR at the card.

Pin	Name	Description
1	VCC	+5 VDC
2	R/W	Read/Write
3	CLOCK	Clock
4	RESET	Reset
5	GND	Ground
6	VPP	+21 VDC
7	I/O	In/Out
8	FUSE	Fuse

SmartCard ISO 7816-2



Pin	Name	Description
1	VCC	+5 VDC
2	RESET	Reset

3	CLOCK	Clock
4	n/c	Not connected
5	GND	Ground
6	n/c	Not connected
7	I/O	In/Out
8	n/c	Not connected

Contributor: Joakim Ogren

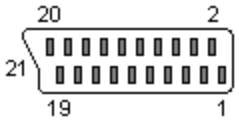
Source: Telecard/Smartcard Technical Spec & Info by Stephane Bausson

Please send any comments to Joakim Ogren.

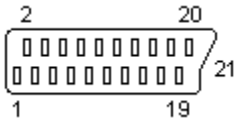
SCART Connector

NEW
NEW
NEW

SCART



(At the video/TV)



(At the cable)

21 PIN SCART FEMALE at the Video/TV.
21 PIN SCART MALE at the Cable.

Pin	Name	Description	Signal Level	Impe
1	AOR	Audio Out Right	0.5 V rms	1k oh
2	AIR	Audio In Right	0.5 V rms	10k o
3	AOL	Audio Out Left + Mono	0.5 V rms	1k oh
4	AGND	Audio Ground		
5	B GND	RGB Blue Ground		
6	AIL	Audio In Left + Mono	0.5 V rms	10k o
7	B	RGB Blue In	0.7 V	75 oh
8	SWTCH	Audio/RGB switch / 16:9		
9	G GND	RGB Green Ground		
10	CLKOUT	Data 2: Clockpulse Out (Unavailble ??)		
11	G	RGB Green In	0.7 V	75 oh
12	DATA	Data 1: Data Out (Unavailble ??)		
13	R GND	RGB Red Ground		
14	DATAGND	Data Ground		
15	R	RGB Red In / Chrominance	0.7 V (Chrom.: 0.3 V burst)	75 oh
16	BLNK	Blanking Signal	1-3 V=RGB, 0-0.4 V=Composite	75 oh
17	VGND	Composite Video Ground		
18	BLNKGND	Blanking Signal Ground		
19	VOUT	Composite Video Out	1 V	75 oh
20	VIN	Composite Video In / Luminance	1 V	75 oh
21	SHIELD	Ground/Shield (Chassis)		

Contributor: Joakim Ogren

Source:Various sources, Video Demystified at Keith Jack's pages

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.mindspring.com/~kjack1/scart.html
Open this address in your WWW browser.

S-Video Connector

NEW
NEW
NEW

S-Video

(At the peripherial)

4 PIN MINI-DIN FEMALE at the peripherial.

Pin	Name	Description
1	GND	Ground (Y)
2	GND	Ground (C)
3	Y	Intensity (Luminance)
4	C	Color (Chrominance)

Contributor: Joakim Ogren

Source:Video Demystified at Keith Jack's pages

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.mindspring.com/~kjack1/svideo.html
Open this address in your WWW browser.

DIN Audio Connector

NEW
NEW
NEW

DIN Audio

NEW (At the peripheral)

NEW (At the cable)

5 PIN DIN 180~ (DIN41524) FEMALE at the peripheral.

5 PIN DIN 180~ (DIN41524) MALE at the cable.

Peripheral	Connected	In L	In R	Out L	Out R	Ground
Amplifier	Pickup, tuner	3	5			2
Amplifier	Taperecorder	3	5	1	4	2
Tuner	Amplifier			3	5	2
Tuner	Taperecorder			1	4	2
Recordplayer	Amplifier			3	5	2
Taperecorder	Amplifier	1	4	3	5	2
Taperecorder	Receiver	1	4	3	5	2
Taperecorder	Microphone	1	4			2

Contributor: Joakim Ogren

Source:ELFA's catalog Nr 44

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.elfa.se
Open this address in your WWW browser.

Turbo LED Connector

NEW
NEW
NEW

Turbo LED

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	+5V	+5 VDC
2	/HS	HighSpeed
3	+5V	+5 VDC

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

AT Backup Battery Connector

NEW
NEW
NEW

AT Backup Battery

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	BATT+	Battery+
2	key	Key
3	GND	Ground
4	GND	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

AT LED/Keylock Connector

NEW
NEW
NEW

AT LED/Keylock

NEW (At the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	LED	LED Power
2	GND	Ground
3	GND	Ground
4	KS	Key Switch
5	GND	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

5.25" Power Connector

NEW
NEW
NEW

5.25" Power

Used for harddisks & 5.25" peripherals.

NEW (At the powersupply cable)

NEW (At the peripheral)

UNKNOWN CONNECTOR at the powersupply cable.

UNKNOWN CONNECTOR at the peripheral.

Pin	Name	Color	Description
1	+5V	Red	+5 VDC
2	GND	Black	+5 V Ground
3	GND	Black	+12 V Ground (Same as +5 V Ground)
4	+12V	Yellow	+12 VDC

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

3.5" Power Connector

NEW
NEW
NEW

3.5" Power

Used for floppies.

NEW (At the powersupply cable)

NEW (At the peripheral)

UNKNOWN CONNECTOR at the powersupply cable.

UNKNOWN CONNECTOR at the peripheral.

Pin	Name	Color	Description
1	+5V	Red	+5 VDC
2	GND	Black	+5 V Ground
3	GND	Black	+12 V Ground (Same as +5 V Ground)
4	+12V	Yellow	+12 VDC

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Motherboard Power Connector

Motherboard Power

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

P8

Pin	Name	Color	Description
1	PG	Orange	Power Good, +5 VDC when all voltages has stabilized.
2	+5V	Red	+5 VDC (or n/c)
3	+12V	Yellow	+12 VDC
4	-12V	Blue	-12 VDC
5	GND	Black	Ground
6	GND	Black	Ground

P9

Pin	Name	Color	Description
1	GND	Black	Ground
2	GND	Black	Ground
3	-5V	White or Yellow	-5 VDC
4	+5V	Red	+5 VDC
5	+5V	Red	+5 VDC
6	+5V	Red	+5 VDC

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

PC Speaker Connector

NEW
NEW
NEW

PC Speaker

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	-SP	-Speaker
2	key	Key
3	GND	Ground
4	+SP5V	+Speaker +5 VDC

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Ethernet 10Base-T Connector

NEW
NEW
NEW

Ethernet 10Base-T

NEW (At the network interface cards)

RJ45 FEMALE CONNECTOR at the network interface cards.

Pin	Name	Description
1	TX+	Trancieve Data+
2	TX-	Trancieve Data-
3	RX+	Recieve Data+
4	n/c	Not connected
5	n/c	Not connected
6	RX-	Recieve Data-
7	n/c	Not connected
8	n/c	Not connected

Note: TX & RX are swapped on Hub's.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

AUI Connector

NEW
NEW
NEW

AUI

Is the directions right???

NEW (At the Ethernet card)

15 PIN D-SUB FEMALE at the Ethernet card.

Pin	Description
1	control in circuit shield
2	control in circuit A
3	data out circuit A
4	data in circuit shield
5	data in circuit A
6	voltage common
7	?
8	control out circuit shield
9	control in circuit B
10	data out circuit B
11	data out circuit shield
12	data in circuit B
13	voltage plus
14	voltage shield
15	?

Contributor: Joakim Ogren

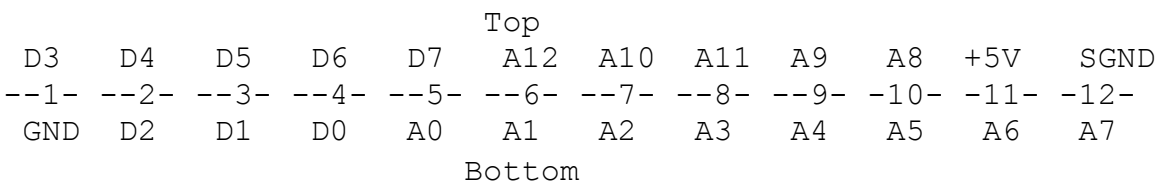
Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

Atari 2600 Cartridge Connector

NEW
NEW
NEW

Atari 2600 Cartridge



NEW (At the Atari)
UNKNOWN CONNECTOR at the Atari.
Connect a 2716 or 2732/2532 EPROM.

Top Row

Pin	2716 Pin	CPU Name	Description
1	13	D3	Data 3
2	14	D4	Data 4
3	15	D5	Data 5
4	16	D6	Data 6
5	17	D7	Data 7
6	*	A12	Address 12
7	19	A10	Address 10
8	n/c	A11	Address 11
9	22	A9	Address 9
10	23	A8	Address 8
11	24	+5V	+5 VDC
12	12	SGND	Shield Ground

* to inverter and back to 18 for chip select

Bottom Row

Pin	2716 Pin	CPU Name	Description
1	1	A7	Address 7
2	2	A6	Address 6
3	3	A5	Address 5
4	4	A4	Address 4
5	5	A3	Address 3
6	6	A2	Address 2
7	7	A1	Address 1
8	8	A0	Address 0
9	9	D0	Data 0
10	10	D1	Data 1
11	11	D2	Data 2
12	n/c	GND	Ground

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ

Please send any comments to Joakim Ogren.

Atari 5200 Cartridge Connector

NEW
NEW
NEW

Atari 5200 Cartridge

NEW (At the Atari)
UNKNOWN CONNECTOR at the Atari.

Pin	Name
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	Enable 80-8F
10	Enable 40-7F
11	Not Connected
12	Ground
13	Ground
14	Ground (System Clock 02 on 2 port)
15	A6
16	A5
17	A2
18	Interlock
19	A0
20	A1
21	A3
22	A4
23	Ground
24	Ground (Video In on 2 port)
25	Ground
26	+5 VDC
27	A7
28	Not Connected
29	A8
30	Audio In (2 port)
31	A9
32	A13
33	A10
34	A12
35	A11
36	Interlock

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ

Please send any comments to Joakim Ogren.

Atari 5200 Expansion Connector

NEW
NEW
NEW

Atari 5200 Expansion

NEW (At the Atari)
UNKNOWN CONNECTOR at the Atari.

Pin	Name
1	+5 VDC
2	Audio Out (2 port)
3	Ground
4	R/W Early
5	Enable E0-EF
6	D6
7	D4
8	D2
9	D0
10	IRQ
11	Ground
12	Serial Data In
13	Serial In Clock
14	Serial Out Clock
15	Serial Data Out
16	Audio In
17	A14
18	System Clock 01
19	A11
20	A7
21	A6
22	A5
23	A4
24	A3
25	A2
26	A1
27	A0
28	Ground
29	D1
30	D3
31	D5
32	D7
33	Not connected
34	Ground
35	Not connected
36	+5 VDC

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ

Please send any comments to Joakim Ogren.

Atari 7800 Cartridge Connector

NEW
NEW
NEW

Atari 7800 Cartridge

NEW (At the Atari)
UNKNOWN CONNECTOR at the Atari.

Pin	Name	Description
1	R/W	Read/Write
2	HALT	Halt
3	D3	Data 3
4	D4	Data 4
5	D5	Data 5
6	D6	Data 6
7	D7	Data 7
8	A12	Address 12
9	A10	Address 10
10	A11	Address 11
11	A9	Address 9
12	A8	Address 8
13	+5V	+5 VDC
14	GND	Ground
15	A13	Address 13
16	A14	Address 14
17	A15	Address 15
18	EAUDIO	EAudio ???
19	A7	Address 7
20	A6	Address 6
21	A5	Address 5
22	A4	Address 4
23	A3	Address 3
24	A2	Address 2
25	A1	Address 1
26	A0	Address 0
27	D0	Data 0
28	D1	Data 1
29	D2	Data 2
30	Gnd	Gnd
31	IRQ	Interrupt
32	CLK2	Clock 2 ???

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ

Please send any comments to Joakim Ogren.

Atari 7800 Expansion Connector

NEW
NEW
NEW

Atari 7800 Expansion

```
 Gnd   +5v  CVideo MLum0 Mlum3 Blank OscDis ExtMen Gnd
--1-- --2--  --3-- --4-- --5-- --6-- --7-- ---8-- --9--

-18-- -17--  -16-- -15-- -14-- -13-- -12-- --11-- -10--
 Gnd  Audio   Rdy   MCol MLum2 MLum1 Msync  Clk2  ExtOsc
```

NEW (At the Atari)
UNKNOWN CONNECTOR at the Atari.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC
3	CVIDEO	Input to RF modulator (Video+Audio)
4	MLUM0	Maria Luminance Bit 0
5	MLUM3	Maria Luminance Bit 3
6	BLANK	Blanking output
7	OSCDIS	Disable 14.31818 MHz Master Clock
8	EXTMEN	External Maria Enable Input
9	GND	Ground
10	EXTOSC	External clock to replace Master Clock
11	CLK2	Phase 2 Clock from the 6502
12	MSYNC	Maria Composite Sync
13	MLUM1	Maria Luminance Bit 1
14	MLUM2	Maria Luminance Bit 2
15	MCOL	Maria Color Phase Angle
16	RDY	Input to the 6502
17	AUDIO	Audio
18	GND	Ground

Contributor: Joakim Ogren

Source:Classic Atari 2600/5200/7800 Game Systems FAQ, Pinout by Harry Dodgson

Please send any comments to Joakim Ogren.

GameBoy Cartridge Connector

NEW
NEW
NEW

GameBoy Cartridge

Available on the Nintendo GameBoy.

NEW (At the GameBoy)
UNKNOWN CONNECTOR at the GameBoy.

Pin	Name	Description
1	VCC	+5 VDC
2	?	? Connected on Gameboy, but not used on GamePaks.
3	/RESET	Reset
4	/WR	Write
5	?	? Used by paging PAL on high capacity GamePaks.
6	A0	Address 0
7	A1	Address 1
8	A2	Address 2
9	A3	Address 3
10	A4	Address 4
11	A5	Address 5
12	A6	Address 6
13	A7	Address 7
14	A8	Address 8
15	A9	Address 9
16	A10	Address 10
17	A11	Address 11
18	A12	Address 12
19	A13	Address 13
20	A14	Address 14
21	/CS	Chip Select
22	D0	Data 0
23	D1	Data 1
24	D2	Data 2
25	D3	Data 3
26	D4	Data 4
27	D5	Data 5
28	D6	Data 6
29	D7	Data 7
30	/RD	Read
31	?	? Connected on Gameboy, but not used on Game-Paks.
32	GND	Ground

Contributor: Joakim Ogren

Source:Nintendo GameBoy FAQ, Pinout by Peter Knight & Josef Mollers

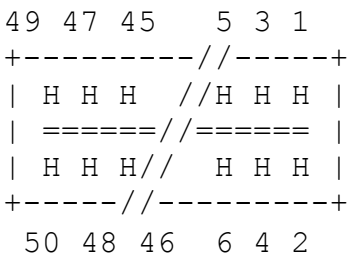
Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.freeflight.com/fms/stuff/gameboy.faq
Open this address in your WWW browser.

MSX Expansion Connector

NEW
NEW
NEW

MSX Expansion



NEW (At the Computer)

50 PIN ?? at the Computer.

Pin	Name	Dir	Description
1	/CS1	NEW	Memory Read in addresses 4000-7FFF
2	/CS2	NEW	Memory Read in addresses 8000-BFFF
3	/CS12	NEW	Memory Read in addresses 4000-BFFF
4	/SLTSL	NEW	Low when Slot 2 (cartridge slot) is selected
5	n/c	-	Not connected.
6	/RFSH	NEW	Refresh signal from CPU
7	/WAIT	NEW	OC, Tells CPU to wait. Refresh signal is not maintained
8	/INT	NEW	OC, Requests a interrupt to CPU (call to addr 38h)
9	/M1	NEW	CPU fetches first part of intruction from memory.
10	/BUSDIR	NEW	NC, was used to control the data direction.
11	/IORQ	NEW	I/O request signal. (Address=Port)
12	/MREQ	NEW	Memory request signal. (Address=Address)
13	/WR	NEW	Write signal (strobe)
14	/RD	NEW	Read signal (strobe)
15	/RESET	NEW	Reset
16	n/c	-	Not connected.
17	A0	NEW	Address 0
18	A1	NEW	Address 1
19	A2	NEW	Address 2
20	A3	NEW	Address 3
21	A4	NEW	Address 4
22	A5	NEW	Address 5
23	A6	NEW	Address 6
24	A7	NEW	Address 7
25	A8	NEW	Address 8
26	A9	NEW	Address 9
27	A10	NEW	Address 10
28	A11	NEW	Address 11
29	A12	NEW	Address 12
30	A13	NEW	Address 13
31	A14	NEW	Address 14
32	A15	NEW	Address 15
33	D0	NEW	Data 0
34	D1	NEW	Data 1
35	D2	NEW	Data 2
36	D3	NEW	Data 3

37	D4	NEW	Data 4
38	D5	NEW	Data 5
39	D6	NEW	Data 6
40	D7	NEW	Data 7
41	GND	NEW	Ground
42	CLOCK	NEW	CPU clock, 3.579 MHz
43	GND	NEW	Ground
44	SW1	-	NC, Insert/remove detection for protection
45	+5V	NEW	+5 VDC (300mA max /slot)
46	SW2	-	NC, Insert/remove detection for protection
47	+5V	NEW	+5 VDC (300mA max /slot)
48	+12V	NEW	+12 VDC (50mA max /slot)
49	SOUNDIN	NEW	Sound input (-5dBm)
50	-12V	NEW	-12 VDC (50mA max /slot)

Note: Direction is Computer relative Peripheral.

Contributor: Joakim Ogren

Source:Mayer's SV738 X'press I/O map

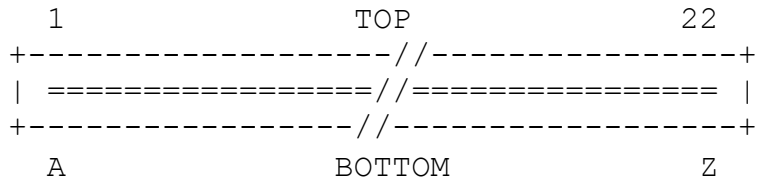
Please send any comments to Joakim Ogren.

Vic 20 Memory Expansion Connector

NEW
NEW
NEW

Vic 20 Memory Expansion

Availble on Commodore Vic 20 computers. On the left side.



NEW (At the Computer)

UNKNOWN CONNECTOR at the Computer.

Pin	Name	Description
A	GND	Ground
B	CA0	Address 0
C	CA1	Address 1
D	CA2	Address 2
E	CA3	Address 3
F	CA4	Address 4
H	CA5	Address 5
J	CA6	Address 6
K	CA7	Address 7
L	CA8	Address 8
M	CA9	Address 9
N	CA10	Address 10
P	CA11	Address 11
R	CA12	Address 12
S	CA13	Address 13
T	I/O 2	Decoded I/O block 2, starting at $9130
U	I/O 3	Decoded I/O block 3, starting at $9140
V	S02	Phase 2 System Clock
W	/NMI	Non maskable Interrupt
X	/RESET	6502 Reset
Y	n/c	Not connected
Z	GND	Ground
1	GND	Ground
2	CD0	Data 0
3	CD1	Data 1
4	CD2	Data 2
5	CD3	Data 3
6	CD4	Data 4
7	CD5	Data 5
8	CD6	Data 6
9	CD7	Data 7
10	/BLK 1	BLK 1 (Memory location $2000 - $3fff)
11	/BLK 2	BLK 2 (Memory location $4000 - $5fff)
12	/BLK 3	BLK 3 (Memory location $6000 - $7fff)
13	/BLK 5	BLK 5 (Memory location $a000 - $bfff)
14	RAM 1	RAM 1 (Memory location $0400 - $07ff)
15	RAM 2	RAM 2 (Memory location $0800 - $0bff)

16	RAM 3	RAM 3 (Memory location $0c00 - $0fff)
17	V R/W	Read/Write from Vic chip (1=R, 0=W)
18	C R/W	Read/Write from CPU (1=R, 0=W)
19	/IRQ	6502 Interrupt Request
20	n/c	Not connected
21	+5V	+5 VDC
22	GND	Ground

Contributor: Joakim Ogren

Sources: Inside your Vic 20 by Ward Shrake
Sources: "The Vic Revealed" by Nick Hampshire, 1982, Hayden Book Co, Inc.
Sources: "Vic20 Programmer's Reference Guide", 1992, Commodore Business, Machines, Inc. and Howard W. Sams & Company, Inc.

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://ccnga.uwaterloo.ca/pub/cbm/vic-20/cartgrab.txt
Open this address in your WWW browser.

This the e-mail address:
wardshrake@aol.com
Choose this address in your e-mail reader.

C64 Cartridge Expansion Connector

NEW
NEW
NEW

C64 Cartridge Expansion

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 Volts DC
3	+5V	+5 Volts DC
4	/IRQ	Interrupt Request
5	/CR/W	
6	DOTCLK	Dot Clock
7	I/O 1	
8	/GAME	Game
9	/EXROM	
10	I/O 2	
11	/ROML	ROM Low
12	BA	
13	/DMA	
14	CD7	Cartridge Data 7
15	CD6	Cartridge Data 7
16	CD5	Cartridge Data 7
17	CD4	Cartridge Data 7
18	CD3	Cartridge Data 7
19	CD2	Cartridge Data 7
20	CD1	Cartridge Data 7
21	CD0	Cartridge Data 7
22	GND	Ground
A	GND	Ground
B	/ROMH	ROM High
C	/RESET	Reset
D	/NMI	Non Maskable Interrupt
E	S02	
F	CA15	Cartridge Address 15
H	CA14	Cartridge Address 14
J	CA13	Cartridge Address 13
K	CA12	Cartridge Address 12
L	CA11	Cartridge Address 11
M	CA10	Cartridge Address 10
N	CA9	Cartridge Address 9
P	CA8	Cartridge Address 8
R	CA7	Cartridge Address 7
S	CA6	Cartridge Address 6
T	CA5	Cartridge Address 5
U	CA4	Cartridge Address 4
V	CA3	Cartridge Address 3
W	CA2	Cartridge Address 2
X	CA1	Cartridge Address 1
Y	CA0	Cartridge Address 0
Z	GND	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

C64 User Port Connector

NEW
NEW
NEW

C64 User Port

NEW (At the computer)
DZM 12 DREH at the computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC (100 mA max)
3	/RESET	Reset
4	CNT1	Counter 1
5	SP1	Serial Port 1
6	CNT2	Counter 2
7	SP2	Serial Port 2
8	/PC2	
9	ATN	Serial Attention In
10	+9V AC	+9 VAC (100 mA max)
11	+9V AC	+9 VAC (100 mA max)
12	GND	Ground
A	GND	Ground
B	/FLAG2	Flag 2
C	PB0	Data 0
D	PB1	Data 1
E	PB2	Data 2
F	PB3	Data 3
H	PB4	Data 4
J	PB5	Data 5
K	PB6	Data 6
L	PB7	Data 7
M	PA2	PA2
N	GND	Ground

Contributor: Joakim Ogren, Nikolas Engstrom

Source:?

Please send any comments to Joakim Ogren.

This the e-mail address:
nikolas.engstrom@pop.landskrona.se
Choose this address in your e-mail reader.

C16/+4 Expansion Bus Connector

NEW
NEW
NEW

C16/+4 Expansion Bus

Availble on Commodore C16 and +4 computers.

NEW (At the Computer)
UNKNOWN CONNECTOR at the Computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC
3	+5V	+5 VDC
4	/IRQ	Interrupt
5	R/W	Read/Write
6	C1HIGH	External Cartridge Chip Selects C1 High
7	C2LOW	External Cartridge Chip Selects C2 Low (reserved)
8	C2HIGH	External Cartridge Chip Selects C2 High (reserved)
9	/CS1	Chip Select 1 ?
10	/CS0	Chip Select 2 ?
11	/CAS	Column Address Strobe
12	MUX	DRAM address multiplex control signal
13	BA	Bus Availble (Low=DMA)
14	D7	Data 7
15	D6	Data 6
16	D5	Data 5
17	D4	Data 4
18	D3	Data 3
19	D2	Data 2
20	D1	Data 1
21	D0	Data 0
22	AEC	?
23	EAI	External Audio In
24	PHI 2	Artificial Phi 2 signal
25	GND	Ground
A	GND	Ground
B	C1LOW	External Cartridge Chip Selects C1 Low
C	/BRESET	?
D	/RAS	Row Address Strobe
E	PHI 0	?
F	A15	Address 15
G	A14	Address 14
H	A13	Address 13
I	A12	Address 12
J	A11	Address 11
K	A10	Address 10
L	A9	Address 9
M	A8	Address 8
N	A7	Address 7
O	A6	Address 6
P	A5	Address 5
Q	A4	Address 4
R	A3	Address 3
S	A2	Address 2

T	A1	Address 1
U	A0	Address 0
V	n/c	Not connected
W	n/c	Not connected
X	n/c	Not connected
Y	GND	Ground

PHI 2: Address valid on the rising edge, data valid on the falling edge

Contributor: Joakim Ogren

Source: Usenet posting in comp.sys.cbm, Pinout specs fort cbm machines needed by Lonnie McClure

Please send any comments to Joakim Ogren.

This the e-mail address:
lmcclure@delphi.com
Choose this address in your e-mail reader.

NEW
NEW
NEW

C16/+4 User Port

Availble on Commodore C16 and +4 computers.

NEW (At the Computer)

UNKNOWN CONNECTOR at the Computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC
3	/BRESET	?
4	P2/CSE	Data 2/Cassette Sense
5	P3	Data 3
6	P4	Data 4
7	P5	Data 5
8	RxC	Recieve Clock
9	ATN	Attention?
10	+9V	+9 VAC
11	+9V	+9 VAC
12	GND	Ground
A	GND	Ground
B	P0	Data 0
C	RxD	Recieve Data
D	RTS	Request to Send
E	DTR	Data Terminal Ready
F	P7	Data 7
G	DCD	Data Carrier Detect
H	P6	Data 6
I	CTS	Clear to Send
J	DSR	Data Set Ready
K	TxD	Transmit Data
L	GND	Ground

Contributor: Joakim Ogren

Source: Usenet posting in comp.sys.cbm, Pinout specs fort cbm machines needed by Lonnie McClure

Please send any comments to Joakim Ogren.

CDTV Diagnostic Slot Connector

NEW
NEW
NEW

CDTV Diagnostic Slot

NEW (At the computer)

80 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	VCC	+5 VDC
4	VCC	+5 VDC
5	/CFGOUT	Configout AutoConfig signal (not connected)
6	/CFGIN	Configin AutoConfig signal (grounded)
7	GND	Ground
8	CCKQ	3.58 MHz CCKQ clock (C3)
9	CDAC	7.16 MHz CDAC clock (90~ before system clock)
10	CCK	3.58 MHz CCK clock (C1)
11	/OVR	Override (Disables /DTACK generation of Gary)
12	XRDY	External Ready (Generates wait states while low).
13	/INT2	Level 2 Interrupt
14	n/c	not connected
15	A5	Address Bus 5
16	/INT6	Level 6 Interrupt
17	A6	Address Bus 6
18	A4	Address Bus 4
19	GND	Ground
20	A3	Address Bus 3
21	A2	Address Bus 2
22	A7	Address Bus 7
23	A1	Address Bus 1
24	A8	Address Bus 8
25	/FC0	Processor Function Code Status (bit 0)
26	A9	Address Bus 9
27	/FC1	Processor Function Code Status (bit 1)
28	A10	Address Bus 10
29	/FC2	Processor Function Code Status (bit 2)
30	A11	Address Bus 11
31	GND	Ground
32	A12	Address Bus 12
33	A13	Address Bus 13
34	/IPL0	Interrupt Priority Level (bit 0)
35	A14	Address Bus 14
36	/IPL1	Interrupt Priority Level (bit 1)
37	A15	Address Bus 15
38	/IPL2	Interrupt Priority Level (bit 2)
39	A16	Address Bus 16
40	/BERR	Bus Error
41	A17	Address Bus 17
42	/VPA	Valid Peripheral Address (asserted by Gary)
43	GND	Ground
44	E	E Clock
45	/VMA	Valid Memory Address (asserted by Gary)

46	A18	Address Bus 18
47	/RST	Reset
48	A19	Address Bus 19
49	/HLT	Halt
50	A20	Address Bus 20
51	A22	Address Bus 22
52	A21	Address Bus 21
53	A23	Address Bus 23
54	/BR	Bus Request
55	GND	Ground
56	/BGACK	Bus Grant Acknowledge
57	D15	Data Bus 15
58	/BG	Bus Grant
59	D14	Data Bus 14
60	/DTACK	Data Transfer Acknowledge (normally asserted by Gary)
61	D13	Data Bus 13
62	R/W	Read/Write (high=read, low=write)
63	D12	Data Bus 12
64	/LDS	Lower Data Strobe
65	D11	Data Bus 11
66	/UDS	Upper Data Strobe
67	GND	Ground
68	/AS	Address Strobe
69	D0	Data Bus 0
70	D10	Data Bus 10
71	D1	Data Bus 1
72	D9	Data Bus 9
73	D2	Data Bus 2
74	D8	Data Bus 8
75	D3	Data Bus 3
76	D7	Data Bus 7
77	D4	Data Bus 4
78	D6	Data Bus 6
79	GND	Ground
80	D5	Data Bus 5

Note: Pin 7-80 is equivalent with the Amiga 500's pin 13-86 at the 86 pin Amiga 500 connector.

Contributor: Joakim Ogren

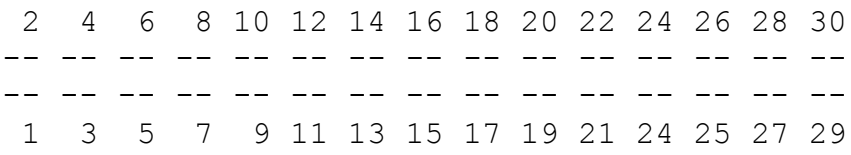
Source:Darren Ewaniuk's CDTV Technical Information

Please send any comments to Joakim Ogren.

CDTV Expansion Slot Connector

NEW
NEW
NEW

CDTV Expansion Slot



NEW (At the computer)

30 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	VCC	+5 VDC
4	VCC	+5 VDC
5	SD1	Data Bus 1
6	SD0	Data Bus 0
7	SD3	Data Bus 3
8	SD2	Data Bus 2
9	SD5	Data Bus 5
10	SD4	Data Bus 4
11	SD7	Data Bus 7
12	SD6	Data Bus 6
13	/SDREQ	DMA Request
14	/INTX	Interrupt Request
15	/CSS	Chip Select
16	/SDACK	DMA Acknowledge
17	/IOR	I/O Read
18	/IOW	I/O Write
19	A8	Address Bus 8
20	7M	7.16 MHz System Clock
21	A6	Address Bus 6
22	A7	Address Bus 7
23	A4	Address Bus 4
24	A5	Address Bus 5
25	A2	Address Bus 2
26	A3	Address Bus 3
27	/IFRST	+5 VDC
28	A1	Address Bus 1
29	GND	Ground
30	GND	Ground

Contributor: Joakim Ogren

Source:Darren Ewaniuk's CDTV Technical Information

Please send any comments to Joakim Ogren.

PC-Engine Cartridge Connector

NEW
NEW
NEW

PC-Engine Cartridge

Availble on the PC Engine.

NEW (At the PC Engine)
UNKNOWN CONNECTOR at the PC Engine.

Pin	Name	Description
1	?	
2	?	
3	A18?	Address 18
4	A16	Address 16
5	A15	Address 15
6	A12	Address 12
7	A7	Address 7
8	A6	Address 6
9	A5	Address 5
10	A4	Address 4
11	A3	Address 3
12	A2	Address 2
13	A1	Address 1
14	A0	Address 0
15	D0	Data 0
16	D1	Data 1
17	D2	Data 2
18	GND	Ground
19	D3	Data 3
20	D4	Data 4
21	D5	Data 5
22	D6	Data 6
23	D7	Data 7
24	/CE	Chip Select
25	A10	Address 10
26	/OE	Output Enable
27	A11	Address 11
28	A9	Address 9
29	A8	Address 8
30	A13	Address 13
31	A14	Address 14
32	A17	Address 17
33	A19?	Address 19
34	R/W	Read/Write
35	?	
36	?	
37	?	
38	+5V	+5 VDC

Pin 1 is the short pin on the left (if the card is to inserted forwards)
Pin 38 is the long pin on the right.

Contributor: Joakim Ogren

Source:Video Games FAQ (Part 3), Pinout by David Shadoff

Please send any comments to Joakim Ogren.

This the e-mail address:

daves@interlog.com

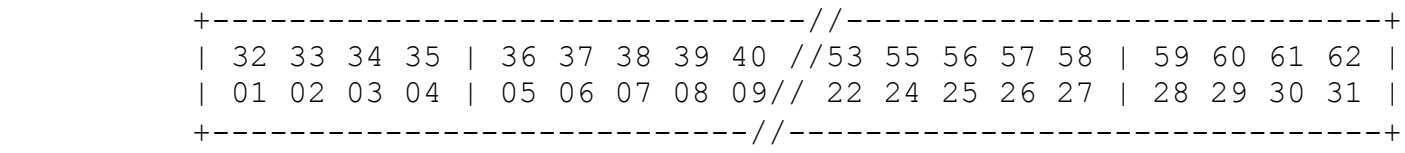
Choose this address in your e-mail reader.

SNES Cartridge Connector

NEW
NEW
NEW

SNES Cartridge

Availble on the Nintendo SNES.



NEW (At the SNES)
UNKNOWN CONNECTOR at the SNES.

Pin	Name	Description
1		
2		
3		
4		
5	GND	Ground
6	A11	Address 11
7	A10	Address 10
8	A9	Address 9
9	A8	Address 8
10	A7	Address 7
11	A6	Address 6
12	A5	Address 5
13	A4	Address 4
14	A3	Address 3
15	A2	Address 2
16	A1	Address 1
17	A0	Address 0
18	/IRQ	Interrupt
19	D0	Data 0
20	D1	Data 1
21	D2	Data 2
22	D3	Data 3
23	/READ	Read
24	CIC	?
25	CIC	?
26	/RAM ENABLE	RAM Enable
27	VCC	+5 VDC
28		
29		
30		
31		
32		
33		
34		
35		
36	GND	Ground
37	A12	Address 12
38	A13	Address 13
39	A14	Address 14

40	A15	Address 15
41	A16	Address 16
42	A17	Address 17
43	A18	Address 18
44	A19	Address 19
45	A20	Address 20
46	A21	Address 21
47	A22	Address 22
48	A23	Address 23
49	/ROM ENABLE	ROM Enable
50	D4	Data 4
51	D5	Data 5
52	D6	Data 6
53	D7	Data 7
54	/WRITE	Write
55	CIC	?
56	CIC	?
57	n/c	Not connected
58	VCC	+5 VDC
59		
60		
61		
62		

Contributor: Joakim Ogren

Source:Video Games FAQ (Part 3), Pinout by Thomas Rolfes

Please send any comments to Joakim Ogren.

This the e-mail address:
rolfes@uni-muenster.de
Choose this address in your e-mail reader.

TG-16 Cartridge Connector

NEW
NEW
NEW

TG-16 Cartridge

Availble on the TG-16.

NEW (At the TG-16)
UNKNOWN CONNECTOR at the TG-16.

Pin	Name	Description
1	?	
2	?	
3	A18?	Address 18
4	A16	Address 16
5	A15	Address 15
6	A12	Address 12
7	A7	Address 7
8	A6	Address 6
9	A5	Address 5
10	A4	Address 4
11	A3	Address 3
12	A2	Address 2
13	A1	Address 1
14	A0	Address 0
15	D7	Data 7
16	D6	Data 6
17	D5	Data 5
18	GND	Ground
19	D4	Data 4
20	D3	Data 3
21	D2	Data 2
22	D1	Data 1
23	D0	Data 0
24	/CE	Chip Select
25	A10	Address 10
26	/OE	Output Enable
27	A11	Address 11
28	A9	Address 9
29	A8	Address 8
30	A13	Address 13
31	A14	Address 14
32	A17	Address 17
33	A19?	Address 19
34	R/W	Read/Write
35	?	
36	?	
37	?	
38	+5V	+5 VDC

Pin 1 is the short pin on the left (if the card is to inserted forwards)
Pin 38 is the long pin on the right.

Contributor: Joakim Ogren

Source:Video Games FAQ (Part 3), Pinout by David Shadoff

Please send any comments to Joakim Ogren.

ZX Spectrum AY-3-8912 Connector

NEW
NEW
NEW

ZX Spectrum AY-3-8912

Can be found at Sinclair ZX Spectrum's, I think

NEW (At the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	SOUND C	Sound C (Can be tied together with A & B)
2	PORT	?
3	VCC	+5 VDC
4	SOUND B	Sound B (Can be tied together with A & C)
5	SOUND A	Sound A (Can be tied together with B & C)
6	GND	Ground
7	PORT	?
8	PORT	?
9	PORT	?
10	PORT	?
11	PORT	?
12	PORT	?
13	PORT	?
14	CLOCK	?
15	CLOCK	?
16	RESET	Reset
17	A8	Address 8?
18	BDIR	?
19	BC2	?
20	BC1	?
21	D7	Data 7
22	D6	Data 6
23	D5	Data 5
24	D4	Data 4
25	D3	Data 3
26	D2	Data 2
27	D1	Data 1
28	D0	Data 0

Contributor: Joakim Ogren

Source:ZX Spectrum FAQ

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://users.ox.ac.uk/~uzdm0006/Damien/speccy/pinouts.html
Open this address in your WWW browser.

ZX Spectrum ULA Connector

NEW
NEW
NEW

ZX Spectrum ULA

Can be found at Sinclair ZX Spectrum's, I think

NEW (At the computer)
UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1		
2	/WR	Write
3	/RD	Read
4	/WE	Write Enable
5	A0	Address 0
6	A1	Address 1
7	A2	Address 2
8	A3	Address 3
9	A4	Address 4
10	A5	Address 5
11	A6	Address 6
12	/INT	Interrupt
13	+5V	+5 VDC (One of the +5V is decoupled through a RC-low-pass.)
14	+5V	+5 VDC (One of the +5V is decoupled through a RC-low-pass.)
15	U	Color-difference signals.
16	V	Color-difference signals.
17	/Y	Inverted Video+Sync.
18	D0	Data 0
19	T0	Keyboard Data 0
20	T1	Keyboard Data 1
21	D1	Data 1
22	D2	Data 2
23	T2	Keyboard Data 2
24	T3	Keyboard Data 3
25	D3	Data 3
26	T4	Keyboard Data 4
27	D4	Data 4
28	SOUND	Analog-I/O-line for beep, save and load.
29	D5	Data 5
30	D6	Data 6
31	D7	Data 7
32	CLOCK	The clock-source to the CPU including the inhibited T-states.
33	/IO-ULA	(A0(CPU) OR /IORQ) for the I/O-port FEh
34	/ROM CS	ROM ChipSelect
35	/RAS	Row Address Strobe
36	A14	Address 14
37	A15	Address 15
38	/MREQ	???
39	Q	The 14 MHz crystal. Other side grounded through capacitor.
40		

Contributor: Joakim Ogren

Source:ZX Spectrum FAQ

Please send any comments to Joakim Ogren.

MIDI Out Connector

NEW
NEW
NEW

MIDI Out

MIDI=Musical Instrument Digital Interface.

NEW (At the peripheral)

NEW (At the cable)

5 PIN DIN 180~ (DIN41524) FEMALE at the peripheral.

5 PIN DIN 180~ (DIN41524) MALE at the cable.

Pin	Name	Description
1	n/c	Not connected
2	GND	Ground
3	n/c	Not connected
4	CSINK	Current Sink
5	CSRC	Current Source

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

MIDI In Connector

NEW
NEW
NEW

MIDI In

MIDI=Musical Instrument Digital Interface.

NEW (At the peripheral)

NEW (At the cable)

5 PIN DIN 180~ (DIN41524) FEMALE at the peripheral.

5 PIN DIN 180~ (DIN41524) MALE at the cable.

Pin	Name	Description
1	n/c	Not connected
2	n/c	Not connected
3	n/c	Not connected
4	CSRC	Current Source
5	CSINK	Current Sink

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Minuteman UPS Connector

NEW
NEW
NEW

Minuteman UPS

Is the directions right???

NEW (At the UPS)

9 PIN D-SUB ??? at the UPS.

Pin	Description
1	Unused
2	Battery power
3	Unused
4	Common (same as 7)
5	Low battery
6	RS-232 level shutdown
7	Common (same as 4)
8	Ground level shutdown (A500 and above, reserved on A500)
9	Reserved

Pins 2 and 5 are connected to Common when they are true.

On pin 6, an rs-232 high level (9V) will shutdown, when running off the battery.

On pin 8, shorting to ground will shutdown.

Contributor: Joakim Ogren

Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

Connector Top 10 Menu

NEW
NEW
NEW

This is not exactly 10 entries, but the most common connectors. I've you don't find what you're searching for here, look at the full list.

What does the the information that is listed for each connector mean? See the tutorial.

Buses:

- ISA NEW - (Technical)
NEW
- EISA - (Technical) NEW
- PCI - (Technical) NEW
- VESA LocalBus (VLB) - (Technical) NEW

In/Out:

- Serial (PC 9)
- Serial (PC 25) NEW
- Parallel (PC)
- Centronics Printer

Video:

- VGA (15)
- VGA (9)
- Amiga Video

Joystick/Mouse:

- Gameport (PC)
- Mouse/Joy (Amiga) NEW

Diskdrive:

- Internal Diskdrive

Keyboard:

- Keyboard (5 PC)
- Keyboard (6 PC)

Data storage interfaces:

- SCSI Internal
- SCSI External Centronics 50
- SCSI External (Amiga/Mac)
- IDE Internal NEW
- ATA Internal NEW

Memories:

- SIMM 30-pin NEW
- SIMM 72-pin NEW

Home audio/video:

- SCART

Networking:

- Ethernet 10Base-T

Last updated 1997-01-19.

Cable Menu

NEW

NEW

What does the the information that is listed for each connector mean? See the tutorial.

Nullmodem:

- Nullmodem (9p to 9p)
- Nullmodem (9p to 25p)
- Nullmodem (25p to 25p)
- Mac to C64 Nullmodem NEW

Modem:

- Modem (9p to 25p)
- Modem (25p to 25p)
- Two-Wire Modem (9p to 25p)
- Two-Wire Modem (25p to 25p)
- Macintosh Modem (With DTR) NEW
- Macintosh Modem (Without DTR) NEW
- Mac to HP48 NEW

Printer:

- Centronics Printercable
- Serial Printer (9p to 25p) NEW
- Serial Printer (25p to 25p) NEW
- C64 Centronics Printer NEW

Parallel:

- LapLink/InterLink Parallel
- ParNet Parallel NEW
- 64NET NEW
- GEOCable NEW

Loopback plugs:

- Parallel Port Loopback
- Serial Port Loopback (9p)
- Serial Port Loopback (25p)

Data storage:

- Floppy cable
- IDE cable
- SCSI cable (Amiga/Mac)
- ST506/412 cable
- ESDI cable

TV/Video/Monitor:

- Video to TV SCART cable
- Amiga to SCART cable

- 9 to 15 pin VGA cable
- Amiga to C1084 Monitor Cable NEW
- C128/C64C to CBM 1902A Monitor Cable NEW

Networking:

- Ethernet 10Base-T Crossover cable
- Ethernet 10Base-T Straight Thru cable

Misc:

- ParaLoad cable
- MIDI cable
- Misc unsupported cables

Last updated 1997-01-19.

Cable Tutorial

NEW

NEW

Short tutorial

Heading

First at each page there a short heading describing the cable.

Pictures of the connectors

After that there is at each page there is one or more pictures of the connectors. Sometimes there is some question marks only. This means that I don't know what kind of connector it is or how it looks.

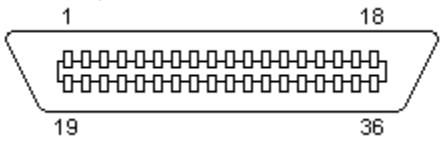
NEW (To the computer)

There may be some pictures I haven't drawn yet. I illustrate this with the following advanced picture:

NEW (To the computer)

Normally are one or more pictures. **These are seen from the front, and NOT the soldside. Holes (female connectors usually) are darkened.** Look at the example below. The first is a female connector and the send a male. The texts insde parentheses will tell you at which kind of the device it will look like that.

NEW (To the Computer)



(To the Printer)

Texts describing the connectors

Below the pictures there is texts that describes the connectors. Including the name of the physical connector.

25 PIN D-SUB MALE to the Computer
36 PIN CENTRONICS MALE to the Printer.

Pin table

The pin table is perhaps the information you're looking for. Should be simple to read. Contains mostly the following three columns; Name, Pin 1, Pin 2. Sometimes when not the same pin is connected to each side there is another column describing the name at connector 2.

	25-DSub	**36-Cen**
Strobe	1	1
Data Bit 0	2	2

Data Bit 1	3	3
Data Bit 2	4	4
Data Bit 3	5	5
Data Bit 4	6	6
Data Bit 5	7	7
Data Bit 6	8	8
Data Bit 7	9	9
...	...	...

Contributor & Source

All persons that helped me or sent me information about the connector will be listed here. The source of the information is perhaps a book or another site. I must admit that I'm bad at writing the source, but I'll try to fill in these in the future.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

NEW

NEW

Nullmodem (9-9) Cable

Use this cable between two DTE devices (for instance two computers).

NEW (To Computer 1).

NEW (To Computer 2).

9 PIN D-SUB FEMALE to Computer 1.

9 PIN D-SUB FEMALE to Computer 2.

	D-Sub 1	D-Sub 2	
Recieve Data	2	3	Transmit Data
Transmit Data	3	2	Recieve Data
Data Terminal Ready	4	6+1	Data Set Ready + Carrier Detect
System Ground	5	5	System Ground
Data Set Ready + Carrier Detect	6+1	4	Data Terminal Ready
Request to Send	7	8	Clear to Send
Clear to Send	8	7	Request to Send

Note: DSR & CD are jumpered to fool the programs to think that their online.

Contributor: Joakim Ogren, Drew Sullivan, Niklas Edmundsson

Source:?

Please send any comments to Joakim Ogren.

This the e-mail address:

drew@ss.org

Choose this address in your e-mail reader.

NEW

NEW

Nullmodem (9-25) Cable

Use this cable between two DTE devices (for instance two computers).

NEW (To Computer 1).

NEW (To Computer 2).

9 PIN D-SUB FEMALE to Computer 1.

25 PIN D-SUB FEMALE to Computer 2.

	D-Sub 9	D-Sub 25	
Recieve Data	2	2	Transmit Data
Transmit Data	3	3	Recieve Data
Data Terminal Ready	4	6+8	Data Set Ready + Carrier Detect
System Ground	5	7	System Ground
Data Set Ready + Carrier Detect	6+1	20	Data Terminal Ready
Request to Send	7	5	Clear to Send
Clear to Send	8	4	Request to Send

Note: DSR & CD are jumpered to fool the programs to think that their online.

Contributor: Joakim Ogren, Drew Sullivan, Niklas Edmundsson

Source:?

Please send any comments to Joakim Ogren.

Nullmodem (25-25) Cable

Use this cable between two DTE devices (for instance two computers).

NEW (To Computer 1).

NEW (To Computer 2).

25 PIN D-SUB FEMALE to Computer 1.

25 PIN D-SUB FEMALE to Computer 2.

	D-Sub 1	D-Sub 2	
Recieve Data	3	2	Transmit Data
Transmit Data	2	3	Recieve Data
Data Terminal Ready	20	6+8	Data Set Ready + Carrier Detect
System Ground	7	7	System Ground
Data Set Ready + Carrier Detect	6+8	20	Data Terminal Ready
Request to Send	4	5	Clear to Send
Clear to Send	5	4	Request to Send

Note: DSR & CD are jumpered to fool the programs to think that their online.

Contributor: Joakim Ogren, Drew Sullivan, Niklas Edmundsson

Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

Mac to C64 Nullmodem Cable

The RS-232 standard on the C64 is a little bit strange. It uses inverted TTL level for the signals. The RS-422 ports on the Macintosh has both an inverted and non-inverted input. By using the inverted instead of non-inverted the inverted C64 level is back to normal.

NEW (At the Computer)

NEW (To the C64).

8 PIN DIN (DIN45326) MALE to the Macintosh.

DZM 12 DREH to the C64 UserPort.

	Mac	**C64**	
GND+RXD-	4+5	1+12+A+N	GND
RXD+	8	M	TXD (PA2)
TXD+	6	B+C	RXD (FLAG2+PB0)
		D+E	RTS+DTR (PB1+PB2)

Contributor: Joakim Ogren

Source: Usenet posting in comp.sys.cbm, A very simple C64 to Macintosh serial cable by Chris Baird

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://stekt.oulu.fi/~jopi/electronics/cbm/C64_to_mac
Open this address in your WWW browser.

This the e-mail address:
mailto:c8923075@cs.newcastle.edu.au
Choose this address in your e-mail reader.

NEW

NEW

Modem (9-25) Cable

This cable should be used for DTE to DCE (for instance computer to modem) connections with hardware handshaking.

NEW (To Computer).

NEW (To Modem).

9 PIN D-SUB FEMALE to the Computer
25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield		1	
Transmit Data	3	2	NEW
Recieve Data	2	3	NEW
Request to Send	7	4	NEW
Clear to Send	8	5	NEW
Data Set Ready	6	6	NEW
System Ground	5	7	
Carrier Detect	1	8	NEW
Data Terminal Ready	4	20	NEW
Ring Indicator	9	22	NEW

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

Modem (25-25) Cable

This cable should be used for DTE to DCE (for instance computer to modem) connections with hardware handshaking.

NEW (To Computer).

NEW (To Modem).

25 PIN D-SUB FEMALE to the Computer
25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield Ground	1	1	
Transmit Data	2	2	NEW
Recieve Data	3	3	NEW
Request to Send	4	4	NEW
Clear to Send	5	5	NEW
Data Set Ready	6	6	NEW
System Ground	7	7	
Carrier Detect	8	8	NEW
Data Terminal Ready	20	20	NEW
Ring Indicator	22	22	NEW

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Two-Wire Modem (9-25) Cable

This cable should be used for DTE to DCE (for instance computer to modem) connections without hardware handshaking.

(To Computer).

(To Modem).

9 PIN D-SUB FEMALE to the Computer
25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield Ground		1	
Transmit Data	3	2	
Recieve Data	2	3	
System Ground	5	7	
Jumper these:			
Request to Send	7		
Clear to Send	8		
Data Set Ready	6		
Carrier Detect	1		
Data Terminal Ready	4		
Request to Send		4	
Clear to Send		5	
Data Set Ready		6	
Carrier Detect		8	
Data Terminal Ready		20	

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Two-Wire Modem (25-25) Cable

This cable should be used for DTE to DCE (for instance computer to modem) connections without hardware handshaking.

(To Computer).

(To Modem).

25 PIN D-SUB FEMALE to the Computer
25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield Ground	1	1	
Transmit Data	2	2	
Recieve Data	3	3	
System Ground	7	7	
Jumper these:			
Request to Send	4		
Clear to Send	5		
Data Set Ready	6		
Carrier Detect	8		
Data Terminal Ready	20		
Request to Send		4	
Clear to Send		5	
Data Set Ready		6	
Carrier Detect		8	
Data Terminal Ready		20	

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

Macintosh Modem (With DTR) Cable

This cable should be used for DTE to DCE (for instance computer to modem) connections with DTR.

NEW (At the Computer)

NEW (To the Modem).

8 PIN DIN (DIN45326) MALE to the Computer.

25 PIN D-SUB MALE to the Modem

	Mac	Dir	Modem	
HSKo	1	NEW	4+20	RTS+DTR
HSKi	2	NEW	5	CTS
TxD-	3	NEW	2	TxD
RxD-	5	NEW	3	RxD
GND+RxD+	4+8	-	7	GND
GPi	5	NEW	8	DCD

Contributor: Joakim Ogren

Source: comp.sys.mac.comm FAQ Part 1

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Macintosh Modem (Without DTR) Cable

This cable should be used for DTE to DCE (for instance computer to modem) connections without DTR.

NEW (At the Computer)

NEW (To the Modem).

8 PIN DIN (DIN45326) MALE to the Computer.
25 PIN D-SUB MALE to the Modem

	Mac	Dir	Modem	
HSKo	1	NEW	4	RTS
HSKi	2	NEW	5	CTS
TxD-	3	NEW	2	TxD
RxD-	5	NEW	3	RxD
GND+RxD+	4+8	-	7	GND
			6+20	DSR+DTR

Contributor: Joakim Ogren

Source: comp.sys.mac.comm FAQ Part 1

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Mac to HP48 Cable

NEW (At the Computer)

NEW (To the HP48).
8 PIN DIN (DIN45326) MALE to the Computer.
4 PIN ??? FEMALE to the HP48

	Mac	**HP48**	
TxD-	3		RxD
RxD-	5		TxD
GND+RxD+	4+8		GND
Shield	SHIELD	SHIELD	Shield

Contributor: Joakim Ogren

Sources: Usenet posting in comp.sys.cbm, Mac to C64 Interface by Tomas Moberg
Sources: Usenet posting in comp.sys.cbm, A very simple C64 to Macintosh serial cable by Chris Baird

Please send any comments to Joakim Ogren.

This the e-mail address:
fr94tmg@ing.umu.se
Choose this address in your e-mail reader.

This the e-mail address:
c8923075@cs.newcastle.edu.au
Choose this address in your e-mail reader.

NEW
NEW
NEW

Printer Cable

NEW (To the Computer)

NEW (To the Printer)

25 PIN D-SUB MALE to the Computer
36 PIN CENTRONICS MALE to the Printer.

	25-DSub	36-Cen
Strobe	1	1
Data Bit 0	2	2
Data Bit 1	3	3
Data Bit 2	4	4
Data Bit 3	5	5
Data Bit 4	6	6
Data Bit 5	7	7
Data Bit 6	8	8
Data Bit 7	9	9
Acknowledge	10	10
Busy	11	11
Paper Out	12	12
Select	13	13
Autofeed	14	14
Error	15	32
Reset	16	31
Select	17	36
Signal Ground	18	33
Signal Ground	19	19
Signal Ground	20	21
Signal Ground	21	23
Signal Ground	22	25
Signal Ground	23	27
Signal Ground	24	29
Signal Ground	25	30

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Serial Printer (9-25) Cable

Use this cable between two a computer (DTE) and a printer (DTE) devices.

NEW (To Computer).

NEW (To Printer).

9 PIN D-SUB FEMALE to Computer.

25 PIN D-SUB FEMALE to Printer.

	D-Sub 1	D-Sub 2	
Recieve Data	3	3	Transmit Data
Transmit Data	2	2	Recieve Data
Clear To Send + Data Set Ready	8 + 6	20	Data Terminal Ready
Carrier Detect + Data Terminal Ready	1 + 4		
Ground	5	7	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Serial Printer (25-25) Cable

Use this cable between two a computer (DTE) and a printer (DTE) devices.

NEW (To Computer).

NEW (To Printer).

25 PIN D-SUB FEMALE to Computer.
25 PIN D-SUB FEMALE to Printer.

	D-Sub 1	D-Sub 2	
Recieve Data	2	3	Transmit Data
Transmit Data	3	2	Recieve Data
Clear To Send + Data Set Ready	5 + 6	20	Data Terminal Ready
Carrier Detect + Data Terminal Ready	8 + 20		
Ground	7	7	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

C64 Centronics Printer Cable

Requires a cartridge with Centronics support (TFCIII or ActionReplay.)

NEW (To the C64).

NEW (To the Printer)

DZM 12 DREH to the C64 UserPort.

36 PIN CENTRONICS MALE to the Printer.

	C64	Dir	Printer	
GND	1,12,A,N	NEW	19-30,33	Ground
FLAG2	B	NEW	10	Acknowledge
PB0	C	NEW	2	Data 0
PB1	D	NEW	3	Data 1
PB2	E	NEW	4	Data 2
PB3	F	NEW	5	Data 3
PB4	H	NEW	6	Data 4
PB5	J	NEW	7	Data 5
PB6	K	NEW	8	Data 6
PB7	L	NEW	9	Data 7
PA2	M	NEW	1	Strobe
GND	3	NEW	31	Initialize Printer

Contributor: Joakim Ogren

Source: CBM Memorial Page Pinouts, pinout by Roy Kannady

Please send any comments to Joakim Ogren.

This the e-mail address:
kannady@pogo.den.mmc.com
Choose this address in your e-mail reader.

NEW
NEW
NEW

LapLink/InterLink Parallel Cable

NEW (To Computer 1).

NEW (To Computer 2).

25 PIN D-SUB MALE to Computer 1.
25 PIN D-SUB MALE to Computer 2.

Name	**Pin**	**Pin**	**Name**
Data Bit 0	2	15	Error
Data Bit 1	3	13	Select
Data Bit 2	4	12	Paper Out
Data Bit 3	5	10	Acknowledge
Data Bit 4	6	11	Busy
Acknowledge	10	5	Data Bit 3
Busy	11	6	Data Bit 4
Paper Out	12	4	Data Bit 2
Select	13	3	Data Bit 1
Error	15	2	Data Bit 0
Reset	16	16	Reset
Select	17	17	Select
Signal Ground	25	25	Signal Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

ParNet Parallel Cable

NEW (To Computer 1).

NEW (To Computer 2).

25 PIN D-SUB MALE to Computer 1.
25 PIN D-SUB MALE to Computer 2.

Name	Pin	Pin	Name
Data Bit 0	2	2	Data Bit 0
Data Bit 1	3	3	Data Bit 1
Data Bit 2	4	4	Data Bit 2
Data Bit 3	5	5	Data Bit 3
Data Bit 4	6	6	Data Bit 4
Data Bit 5	7	7	Data Bit 5
Data Bit 6	8	8	Data Bit 6
Data Bit 7	9	9	Data Bit 7
Acknowledge + Select	10+13	10+13	Acknowledge + Select
Busy	11	11	Busy
Paper Out	12	12	Paper Out
Signal Ground	17-25	17-25	Signal Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

64NET Cable

NEW (To C64).

NEW (To PC).

DZM 12 DREH to the C64 UserPort.
25 PIN D-SUB MALE to the PC

	C64	Dir	PC	
GND	A	NEW	25	GND
PB0	C	NEW	10	/ACK
PB1	D	NEW	11	BUSY
PB2	E	NEW	12	PE
PB3	F	NEW	5	D3
PB4	H	NEW	6	D4
PB5	J	NEW	7	D5
PB6	K	NEW	8	D6
PB7	L	NEW	9	D7

Contributor: Joakim Ogren

Source: 64NET v1.82.58 documentation by Paul Gardner-Stephen

Please send any comments to Joakim Ogren.

This the e-mail address:
gardners@ist.flinders.edu.au
Choose this address in your e-mail reader.

NEW
NEW
NEW

GEOCable Cable

NEW (To the C64).

NEW (To the Printer)
DZM 12 DREH to the C64 UserPort.
36 PIN CENTRONICS MALE at the Printer.

	C64	Printer	
Ground	A	33	Ground
Flag 2	B	11	Busy
PB0	C	2	Data 1
PB1	D	3	Data 2
PB2	E	4	Data 3
PB3	F	5	Data 4
PB4	H	6	Data 5
PB5	J	7	Data 6
PB6	K	8	Data 7
PB7	L	9	Data 8
PA2	M	1	Strobe
Ground	N	16	Ground

Contributor: Joakim Ogren

Source: comp.sys.cbm General FAQ v3.1 Part 7

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Parallel Port Loopback

Used to verify that a port is working. This one works with Norton Utilities: Norton Diagnostics from Symantec.

NEW (To Computer).

25 PIN D-SUB MALE to Computer.

Name	Pin	Pin	Name
Data Bit 0	2	15	Error
Data Bit 1	3	13	Select
Data Bit 2	4	12	Paper Out
Data Bit 3	5	10	Acknowledge
Data Bit 4	6	11	Busy

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Serial Port Loopback (9)

Used to verify that a port is working. This one works with Norton Utilities: Norton Diagnostics from Symantec.

NEW (To Computer).

9 PIN D-SUB FEMALE to Computer.

Name	Pin	Pin	Pin	Pin
Jumpering 1	2	3		
Jumpering 2	7	8		
Jumpering 3	1	4	6	9

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Serial Port Loopback (25)

Used to verify that a port is working. This one works with Norton Utilities: Norton Diagnostics from Symantec.

NEW (To Computer).

25 PIN D-SUB FEMALE to Computer.

Name	**Pin**	**Pin**	**Pin**	**Pin**
Jumpering 1	2	3		
Jumpering 2	4	5		
Jumpering 3	6	8	20	22

Contributor: Joakim Ogren

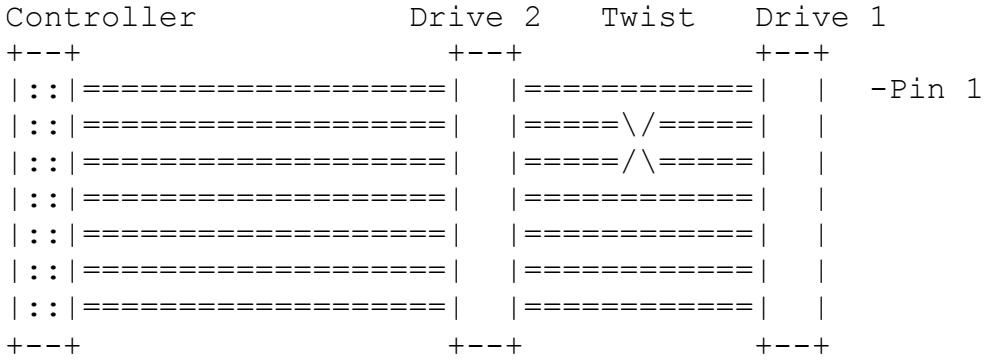
Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Floppy Cable

The original floppy cable required that each drive was jumpered to the right ID. But IBM come up with an idea to avoid jumpering the floppies.
If wire 10-16 are twisted before the last connector the jumpering is avoided. Each drive should be jumpered to act as Drive 2. If only one drive is used then leave the middle connector free.
The IDC could also be an edge connector on some old drives.



NEW (To the Controller)

NEW (To the Drive 2)

NEW (To the Drive 1)

34 PIN IDC FEMALE to the Controller.
34 PIN IDC FEMALE to the Drive 2.
34 PIN IDC FEMALE to the Drive 1.

	Controller	**Drive 1**	**Drive 2**
Wire 1-9	1-9	1-9	1-9
Wire 10	10	16	10
Wire 11	11	15	11
Wire 12	12	14	12
Wire 13	13	13	13
Wire 14	14	12	14
Wire 15	15	11	15
Wire 16	16	10	16
Wire 17-34	17-34	17-34	17-34

Contributor: Joakim Ogren

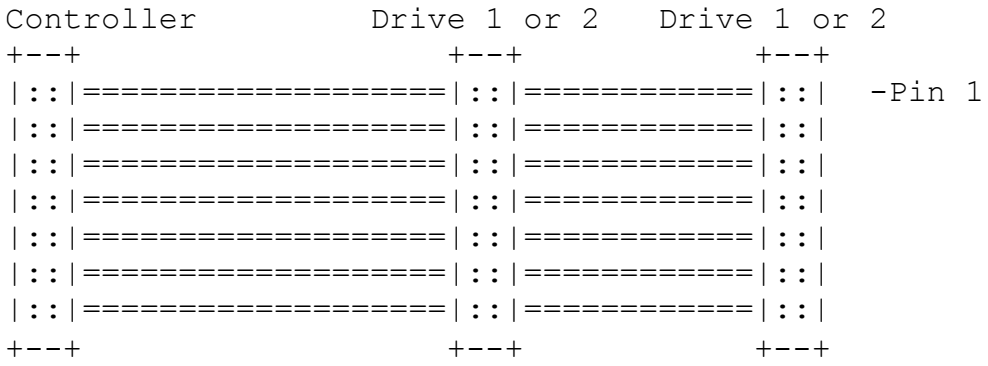
Source: TheRef TechTalk

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

IDE Cable

The IDE interface requires only one cable. All pins straight from 1 to 1, 2 to 2 and so on. The drives can be connected in any order. Only remember that one should be jumpered as Master and the other as Slave. If only one drive is used, jumper it as Single (if such a mode exists, or most common Master else).



NEW (To the Controller)

NEW (To the Drive 1)

NEW (To the Drive 2)

40 PIN IDC FEMALE to the Controller.
40 PIN IDC FEMALE to the Drive 1.
40 PIN IDC FEMALE to the Drive 2.

	Controller	**Drive 1**	**Drive 2**
Wire 1-40	1-40	1-40	1-40

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

SCSI Cable (Amiga/Mac)

NEW (To the Amiga/Mac).

NEW (To the Peripherial).

25 PIN D-SUB FEMALE to the Amiga/Mac.
50 PIN IDC FEMALE to the Peripherial.

	DSub	IDC
Request	1	48
Message	2	42
Input/Output	3	50
Reset	4	40
Acknowledge	5	38
Busy	6	36
Data Bus 0	8	2
Data Bus 3	10	8
Data Bus 5	11	12
Data Bus 6	12	14
Data Bus 7	13	16
Control/Data	15	46
Attention	17	32
Select	19	44
Data Parity	20	18
Data Bus 1	21	4
Data Bus 2	22	6
Data Bus 4	23	10
Termination Power	25	26

Note: All the other pins (7+9+14+16+18+24) at the DSub should be connected to the all odd pins except 25 at the IDC connector.

Contributor: Joakim Ogren

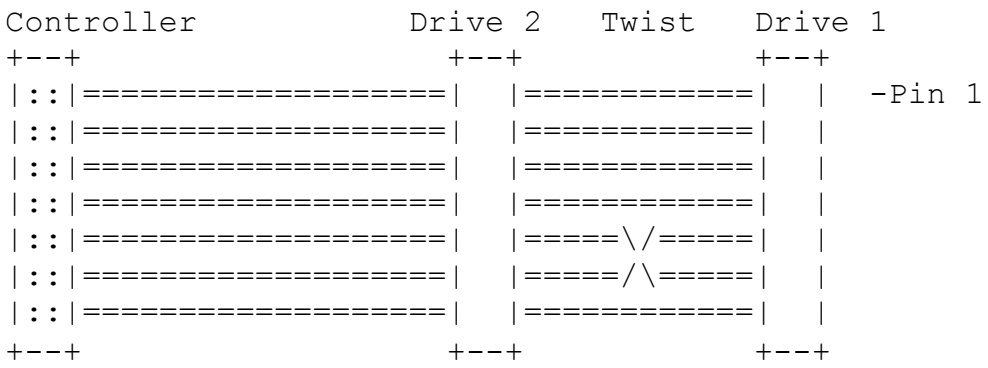
Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

ST506/412 Cable

The ST506/412 interface requires two cables, one for control and one for data. The control cable is shared between the two drives. But each drive has each own data cable. By twisting some wires on the control cable it won't be nescessary to set the ID for each drive, since the twist will do the job. Wires 25 to 29 should be twisted between drive 1 & drive 2.



Control cable

NEW (To the Controller)

NEW (To the Drive 2)

NEW (To the Drive 1)

34 PIN IDC FEMALE to the Controller.
34 PIN IDC FEMALE to the Drive 2.
34 PIN IDC FEMALE to the Drive 1.

	Controller	Drive 1	Drive 2
Wire 1-24	1-9	1-9	1-9
Wire 25	25	29	25
Wire 26	26	28	26
Wire 27	27	27	27
Wire 28	28	26	28
Wire 29	29	25	29
Wire 30-34	30-34	30-34	30-34

Data cable

NEW (To the Controller)

NEW (To the Drive)

20 PIN IDC FEMALE to the Controller.
20 PIN IDC FEMALE to the Drive.

	Controller	Drive
Wire 1-20	1-20	1-20

Contributor: Joakim Ogren

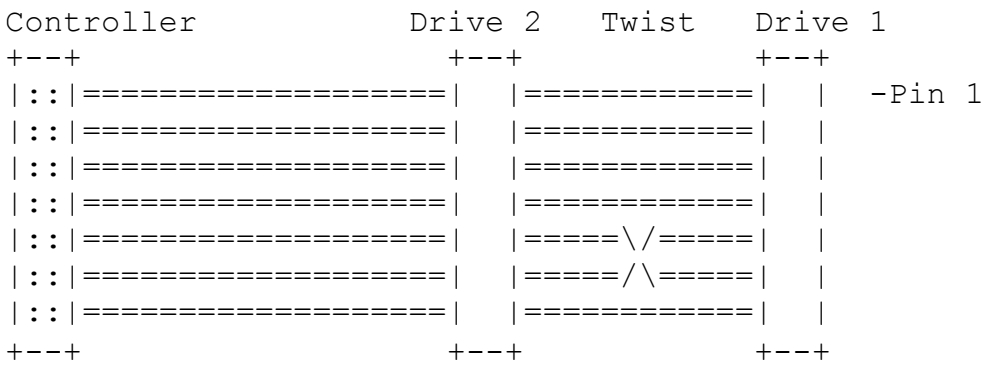
Source: TheRef TechTalk

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

ESDI Cable

The ESDI interface requires two cables, one for control and one for data. The control cable is shared between the two drives. But each drive has each own data cable. By twisting some wires on the control cable it won't be nescessary to set the ID for each drive, since the twist will do the job. Wires 25 to 29 should be twisted between drive 1 & drive 2.



Control cable

NEW (To the Controller)

NEW (To the Drive 2)

NEW (To the Drive 1)

34 PIN IDC FEMALE to the Controller.
34 PIN IDC FEMALE to the Drive 2.
34 PIN IDC FEMALE to the Drive 1.

	Controller	Drive 1	Drive 2
Wire 1-24	1-9	1-9	1-9
Wire 25	25	29	25
Wire 26	26	28	26
Wire 27	27	27	27
Wire 28	28	26	28
Wire 29	29	25	29
Wire 30-34	30-34	30-34	30-34

Data cable

NEW (To the Controller)

NEW (To the Drive)

20 PIN IDC FEMALE to the Controller.
20 PIN IDC FEMALE to the Drive.

	Controller	Drive
Wire 1-20	1-20	1-20

Contributor: Joakim Ogren

Source: TheRef TechTalk

Please send any comments to Joakim Ogren.

Video to TV SCART Cable

NEW
NEW
NEW

Video to TV SCART cable

NEW (To the TV)

NEW (To the Video Recorder)

21 PIN SCART MALE to the TV.

21 PIN SCART MALE to the Video Recorder.

	TV	VCR	
Audio Right Out	1	2	Audio Right In
Audio Right In	2	1	Audio Right Out
Audio Left Out	3	6	Audio Left In
Audio Left In	6	3	Audio Left Out
Audio Ground	4	4	Audio Ground
Red	15	15	Red
Red Ground	13	13	Red Ground
Green	11	11	Green
Green Ground	9	9	Green Ground
Blue	7	7	Blue
Blue Ground	5	5	Blue Ground
Status / 16:9	8	8	Status / 16:9
Reserved	10	10	Reserved
Reserved	12	12	Reserved
Fast Blanking Ground	14	14	Fast Blanking Ground
Fast Blanking	16	16	Fast Blanking
Video Out Ground	17	18	Video In Ground
Video In Ground	18	17	Video Out Ground
Video Out	19	20	Video In
Video In Ground	20	19	Video Out
Ground	21	21	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Amiga to SCART Cable

NEW
NEW
NEW

Amiga to SCART cable

NEW (To the Amiga)

NEW (To the TV)

23 PIN D-SUB FEMALE to the Amiga

21 PIN SCART MALE to the TV

	Amiga	TV	
Analog Red	3	15	RGB Red In
Analog Green	4	11	RGB Green In
Analog Blue	5	7	RGB Blue In
Composite Sync	10	20	Video In
Video GND	17	17	Video GND
GND	19	18	Blanking GND
+12V	22	16	Blanking (Connect via a 150 Ohm resistor)
+12V	22	8	Audio/RGB switch (Connect via a 1 kOhm resistor)
Phono Right		2	Audio IN Right
Phono Right GND		4	GND
Phono Left		6	Audio IN Left
Phono Left GND		4	GND

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

9 to 15 pin VGA Cable

NEW
NEW
NEW

9 to 15 pin VGA cable

NEW (To the Computer)

NEW (To the Monitor)

9 PIN D-SUB MALE to the Computer

15 PIN HIGHDENSITY D-SUB FEMALE to the Monitor

	9-Pin	**15-Pin**
Red Video	1	1
Green Video	2	2
Blue Video	3	3
Horizontal Sync	4	13
Vertical Sync	5	14
Red GND	6	6
Green GND	7	7
Blue GND	8	8
Sync GND	9	10 + 11

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Amiga to C1084 Monitor Cable

NEW (To the Amiga)

NEW (At the Monitor)
23 PIN D-SUB FEMALE to the Amiga.
6 PIN DIN MALE at the Monitor.

	Amiga	C1084	
R	3	4	R
G	4	1	G
B	5	5	B
SYNC	10	2	HSYNC
GND	16	3	GND

Contributor: Joakim Ogren

Source: Usenet posting in sfnet.harrastus.elektroniikka, Philips 1084 monarin kytkenta by Kari Hautanen

Please send any comments to Joakim Ogren.

This the e-mail address:
kari.hautanen@compart.fi
Choose this address in your e-mail reader.

NEW
NEW
NEW

C128/C64C to CBM 1902A Monitor Cable

NEW (At the Computer)

NEW (At the Monitor)

8 PIN DIN (DIN45326) MALE at the Computer.
6 PIN DIN MALE at the Monitor.

	Computer	C1902A	
LUM	1	6	LUM
CHROMA	8	4	CHROMA
GND	2	3	GND
AOUT	3	2	AUDIO

Contributor: Joakim Ogren

Source: cbm.comp.sys General FAQ v3.1 Part 7

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Ethernet 10Base-T Crossover Cable

NEW (To network interface card 1).

NEW (To network interface card 2).

RJ45 MALE to network interface card 1).

RJ45 MALE to network interface card 2).

This cable can be used to cascade hubs, or for connecting two Ethernet stations back-to-back without a hub.

Name	Pin	Pin	Name
TX+	1	3	RX+
TX-	2	6	RX-
RX+	3	1	TX+
RX-	6	2	TX-

Contributor: Joakim Ogren, Jim C?, Jason D. Pero

Source:?

Please send any comments to Joakim Ogren.

This the e-mail address:

jimc@megalink.net

Choose this address in your e-mail reader.

This the e-mail address:
JDP6640@ritvax.isc.rit.edu
Choose this address in your e-mail reader.

NEW
NEW
NEW

Ethernet 10Base-T Straight Thru Cable

NEW (To network interface card).

NEW (To hub).

RJ45 MALE to network interface card).

RJ45 MALE to hub).

Name	Pin	Cable Color	Pin	Name
TX+	1	White/Orange	1	TX+
TX-	2	Orange	2	TX-
RX+	3	White/Green	3	RX+
	4	Blue	4	
	5	White/Blue	5	
RX-	6	Green	6	RX-
	7	White/Brown	7	
	8	Brown	8	

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

ParaLoad Cable

NEW (To C64).

NEW (To Amiga).
DZM 12 DREH at the C64 UserPort.
25 PIN D-SUB MALE at the Amiga

	C64	Amiga	
Ground	A	17-25	Ground
FLAG2	B	1	Strobe
PB0	C	2	D0
PB1	D	3	D1
PB2	E	4	D2
PB3	F	5	D3
PB4	H	6	D4
PB5	J	7	D5
PB6	K	8	D6
PB7	L	9	D7
PA2	M	11	Busy

Contributor: Joakim Ogren

Source: ParaLoad documentation

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

MIDI Cable

NEW (To the 1st peripheral)

NEW (To the 2nd peripheral)

5 PIN DIN 180~ (DIN41524) MALE to the 1st peripheral.

5 PIN DIN 180~ (DIN41524) MALE to the 1st peripheral.

	1st	**2nd**
Shield	2	2
Current Source	4	4
Current Sink	5	5

Note: Although that pin 2 only is connected at MIDI Out it's simpler to connect it to both ends.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Misc unsupported Cables

These cables may or may not be correctly constructed. Handle with care.

Amiga to IBM RGBI Cable

NEW (To the Monitor).

NEW (To the Amiga).
9 PIN D-SUB ?? to the Monitor.
23 PIN D-SUB FEMALE to the Amiga.

	9 Pin	23 Pin	Comment
Ground	1	16	
Ground	2	16	
Digital Red	3	9	(Via 2 Hex Inverters, i.e 74LS04)
Digital Green	4	8	(Via 2 Hex Inverters, i.e 74LS04)
Digital Blue	5	9	(Via 2 Hex Inverters, i.e 74LS04)
Digital Intensity	6	6	(Via 2 Hex Inverters, i.e 74LS04)
Horizontal Sync	8	11	(Via 1 Hex Inverters, i.e 74LS04)
Verical Sync	9	12	(Via 1 Hex Inverters, i.e 74LS04)
+5V		23	(Power for the IC)

C128 80 columns to 1702 monitor Cable

NEW (To the C128).

NEW (To the C1702).
9 PIN D-SUB MALE to the C128.
PHONO MALE to the Monitor.

	C128	C1702	
Ground	1	1	Ground
Monochrome out	7	2	Signal

Contributor: Joakim Ogren

Source: Gordon

Please send any comments to Joakim Ogren.

This the e-mail address:

GAJ2@psuvm.psu.edu

Choose this address in your e-mail reader.

Adapter Menu

NEW

NEW

What does the the information that is listed for each adapter mean? See the tutorial.

Serial:

- Nullmodem adapter
- 9p to 25p Serial adapter

Keyboard:

- Mini-DIN to DIN Keyboard adapter
- DIN to Mini-DIN Keyboard adapter
- PS-2 Keyboard (Gateway) Y Adapter NEW
- PS-2 Keyboard (IBM Thinkpad) Y Adapter NEW

Joysticks:

- Amiga 4 Joysticks adapter
- PC 2 Joysticks adapter

Misc:

- A1000 to Amiga Parallel adapter

Last updated 1997-01-19.

Adapter Tutorial

NEW 

NEW

Short tutorial

Heading

First at each page there a short heading describing the adapter.

Pictures of the connectors

After that there is at each page there is one or more pictures of the connectors, usually there's two connectors. Sometimes there is some question marks only. This means that I don't know what kind of connector it is or how it looks.

NEW (To the computer)
There may be some pictures I haven't drawn yet. I illustrate this with the following advanced picture:
NEW (To the computer)
Normally are one or more pictures. **These are seen from the front, and NOT the soldside. Holes (female connectors usually) are darkened.** Look at the example below. The first is a female connector and the send a male. The texts insde parentheses will tell you at which kind of the device it will look like that.
NEW (To the Computer).

NEW (To the Serialcable).

Texts describing the connectors

Below the pictures there is texts that describes the connectors. Including the name of the physical connector.

9 PIN D-SUB FEMALE to the Computer.
25 PIN D-SUB MALE to the Serialcable.

Pin table

The pin table is perhaps the information you're looking for. Should be simple to read. Contains mostly the following three columns; Name, Pin 1, Pin 2. Sometimes when not the same pin is connected to each side there is another column describing the name at connector 2.

	9-Pin	25-Pin
Carrier Detect	1	8
Recieve Data	2	3
Transmit Data	3	2
Data Terminal Ready	4	20
System Ground	5	7
Data Set Ready	6	6

Request to Send	7	4
Clear to Send	8	5
Ring Indicator	9	22

Contributor & Source

All persons that helped me or sent me information about the connector will be listed here. The source of the information is perhaps a book or another site. I must admit that I'm bad at writing the source, but I'll try to fill in these in the future.

Contributor: Joakim Ogren

Source:Amiga 4000 User's Guide from Commodore

NEW

NEW

Nullmodem Adapter

This adapter will enable you to use a normal serialcable as a nullmodem.

NEW (To the Computer).

NEW (To the Serialcable).

25 PIN D-SUB FEMALE to the Computer.

25 PIN D-SUB MALE to the Serialcable.

	Female	Male	
Shield Ground	1	1	Shield Ground
Transmit Data	2	3	Recieve Data
Recieve Data	3	2	Transmit Data
Request to Send	4	5	Clear to Send
Clear to Send	5	4	Request to Send
Data Set Ready	6	20	Data Terminal Ready
Data Terminal Ready	20	6	Data Set Ready
Ground	7	7	Ground

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

9 to 25 Serial Adapter

This adapter will enable you to connect a 25 pin serialcable to a 9 pin connector at the computer.

NEW (To the Computer).

NEW (To the Serialcable).

9 PIN D-SUB FEMALE to the Computer.

25 PIN D-SUB MALE to the Serialcable.

	9-Pin	25-Pin
Carrier Detect	1	8
Recieve Data	2	3
Transmit Data	3	2
Data Terminal Ready	4	20
System Ground	5	7
Data Set Ready	6	6
Request to Send	7	4
Clear to Send	8	5
Ring Indicator	9	22

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

Mini-DIN to DIN Keyboard Adapter

This adapter will enable you to use a keyboard with a 6 pin Mini-DIN connector to a computer with a 5 pin DIN connector.

NEW (To the keyboard)

NEW (To the computer)

6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the keyboard.

5 PIN DIN 180~ (DIN41524) MALE to the computer.

	Mini-DIN	**DIN**
Shield	Shield	Shield
Data	1	2
Ground	3	4
+5 VDC	4	5
Clock	5	1

Contributor: Joakim Ogren, Gilles Ries

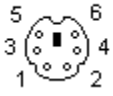
Source:?

Please send any comments to Joakim Ogren.

DIN to Mini-DIN Keyboard Adapter

This adapter will enable you to use a keyboard with a 5 pin DIN connector to a computer with a 6 pin Mini-DIN connector.

NEW (To the keyboard)



(To the computer)

5 PIN DIN 180~ (DIN41524) FEMALE to the keyboard.

6 PIN MINI-DIN MALE (PS/2 STYLE) to the computer.

	DIN	**Mini-DIN**
Shield	Shield	Shield
Clock	1	5
Data	2	1
Ground	4	3
+5 VDC	5	4

Contributor: Joakim Ogren, Gilles Ries

Source:?

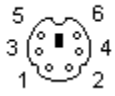
Please send any comments to Joakim Ogren.

NEW

NEW

PS/2 Keyboard (Gateway) Y Adapter

This adapter will enable you to use a keyboard and mouse at the same time. For Gateway computer, may work with other computers (Let me know).



(To the Computer)

NEW (To the Keyboard)

NEW (To the Mouse)

6 PIN MINI-DIN MALE (PS/2 STYLE) to the Computer.
6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Keyboard.
6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Mouse.

Computer	Keyboard	Mouse
1	2	-
2	-	2
3	3	3
4	4	4
5	6	-
6	-	6

Contributor: Joakim Ogren, Gilles Ries

Source: Tommy's pinout Collection by Tommy Johnson

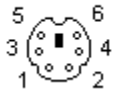
Please send any comments to Joakim Ogren.

NEW

NEW

PS/2 Keyboard (IBM Thinkpad) Y Adapter

This adapter will enable you to use a keyboard and mouse at the same time. For IBM Thinkpad computer, may work with other computers (Let me know).



(To the Computer)

NEW (To the Keyboard)

NEW (To the Mouse)

6 PIN MINI-DIN MALE (PS/2 STYLE) to the Computer.
6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Keyboard.
6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Mouse.

Computer	Keyboard	Mouse
1	2	-
2	-	1,2
3	3	3
4	4	4
5	6	5
6	-	6

Contributor: Joakim Ogren, Gilles Ries

Source: Tommy's pinout Collection by Tommy Johnson

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Amiga 4 Joysticks adapter

This adapter will make it possible to connecto 2 extra joysticks to the Amiga. This requires that the game is aware of this Multi-Joystick Extender in order to use it.

NEW (To the 1st Joystick).

NEW (To the 2nd Joystick).

NEW (To the Computer).

9 PIN D-SUB MALE to the 1st Joystick.
9 PIN D-SUB MALE to the 2nd Joystick.
25 PIN D-SUB MALE to the Serialcable.

	Parport	**Joy 1**	**Joy 2**
Up 1	2	1	
Down 1	3	2	
Left 1	4	3	
Right 1	5	4	
Up 2	6		1
Down 2	7		2
Left 2	8		3
Right 2	9		4
Fire 2	11		6
Fire 1	13	6	
Ground 2	18		8
Ground 1	19	8	

Contributor: Joakim Ogren

Source: Tomi Engdahl's Joystick page

Please send any comments to Joakim Ogren.

This is the URL for the WWW page:
http://www.hut.fi/~then/circuits/joystick.html
Open this address in your WWW browser.

NEW
NEW
NEW

PC 2 Joysticks adapter

This adapter will make it possible to connect 1 extra joystick to the PC. The gameport contains pins for two joysticks but you'll need this adapter to be able to connect two joysticks to one connector.

NEW (To the Computer)

NEW (To the 1st Joystick)

NEW (To the 2nd Joystick)

15 PIN D-SUB MALE to the Computer.
15 PIN D-SUB FEMALE to the 1st Joystick.
15 PIN D-SUB FEMALE to the 2nd Joystick.

	PC	Joy 1	Joy 2
+5 VDC	1	1	-
Button 1	2	2	
Joystick 1 - X	3	3	
Ground	4	4	4
Ground	5	5	5
Joystick 1 - Y	6	6	
Button 2	7	7	
+5 VDC	8	8	
+5 VDC	9	9	1
Button 4	10	10	2
Joystick 2 - X	11	11	3
Ground	12	12	
Joystick 2 - Y	13	13	6
Button 3	14	14	7
+5 VDC	15	15	8

Note: Since pin 12 is offen used for MIDI-signals on gameport equipped soundcards it's better to use the ground from pin 4 & 5, pin 15 is also used for MIDI-signals...

Contributor: Joakim Ogren

Source: Tomi Engdahl's Joystick page

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

A1000 to Amiga Parallel Adapter

This adapter will enable you to connect normal Amiga peripherials to an Amiga 1000. The Amiga 1000 has a male connector at the computer instead of a normal female connector. And some signals has changed places.

NEW (To the Amiga 1000).

NEW (To the Amiga peripherial).

25 PIN D-SUB FEMALE to the Amiga 1000.

25 PIN D-SUB FEMALE to the Amiga peripherial.

	A1000	**Amiga**
Ground	14	23
Ground	15	24
Ground	16	25
+5V	23	14
n/c	24	15
Reset	25	16

All other straight over, 1 to 1, 2 to 2...

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Misc Menu

NEW

NEW

Active Filters:

- Butterworth 1st order Lowpass
- Butterworth 1st order Highpass
- Butterworth 2nd order Lowpass
- Butterworth 2nd order Highpass
- Butterworth 3rd order Lowpass
- Butterworth 3rd order Highpass
- Butterworth 4th order Lowpass
- Butterworth 4th order Highpass
- Bessel 2nd order Lowpass
- Bessel 2nd order Highpass
- Bessel 3rd order Lowpass
- Bessel 3rd order Highpass
- Bessel 4th order Lowpass
- Bessel 4th order Highpass
- Linkwitz 4th order Lowpass
- Linkwitz 4th order Highpass

Definitions:

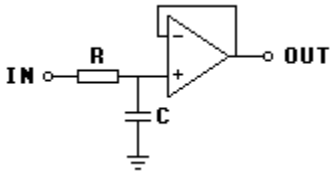
- DTE & DCE

Last updated 1997-01-19.

NEW

NEW

Active Filter: Butterworth (1st order, 6 dB/octave, Lowpass)



R=4.7k-10 kOhm
C=1.000/(2*pi*Fc*R)

Contributor: Joakim Ogren

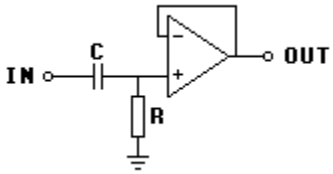
Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

Active Filter: Butterworth (1st order, 6 dB/octave, Highpass)



C=4.7n-10nF
R=1.000/(2*pi*Fc*C)

Contributor: Joakim Ogren

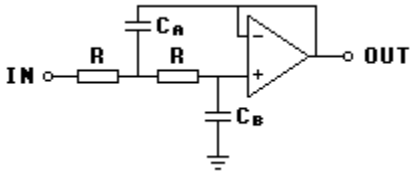
Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

Active Filter: Butterworth (2nd order, 12 dB/octave, Lowpass)



R=4.7k-10 kOhm
Ca=1.414/(2*pi*Fc*R)
Cb=0.7071/(2*pi*Fc*R)

Contributor: Joakim Ogren

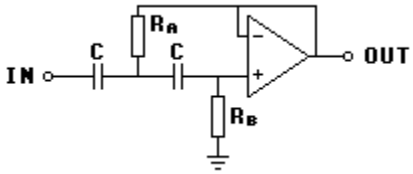
Source:?

Please send any comments to Joakim Ogren.

NEW

NEW

Active Filter: Butterworth (2st order, 12 dB/octave, Highpass)



C=4.7n-10nF
Ra=0.7071/(2*pi*Fc*C)
Rb=1.414/(2*pi*Fc*C)

Contributor: Joakim Ogren

Source:?

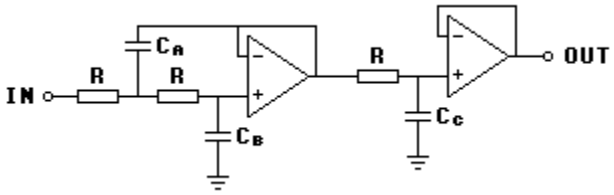
Please send any comments to Joakim Ogren.

NEW

MISC

NEW

Active Filter: Butterworth (3st order, 18 dB/octave, Lowpass)



R=4.7k-10 kOhm
Ca=2.000/(2*pi*Fc*R)
Cb=0.500/(2*pi*Fc*R)
Cc=1.000/(2*pi*Fc*R)

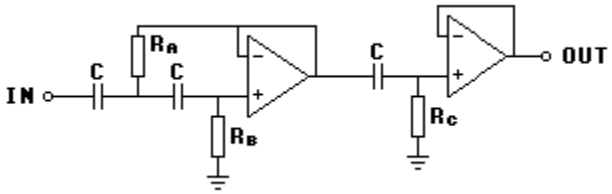
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Butterworth (3st order, 18 dB/octave, Highpass)



C=4.7n-10nF
Ra=0.500/(2*pi*Fc*C)
Rb=2.000/(2*pi*Fc*C)
Rc=1.000/(2*pi*Fc*C)

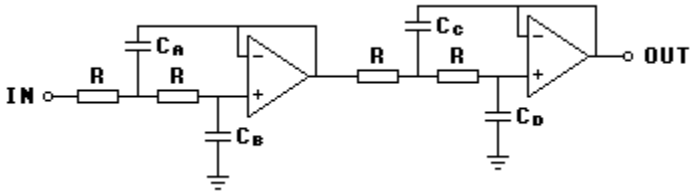
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Butterworth (4th order, 24 dB/octave, Lowpass)



R=4.7k-10 kOhm
Ca=1.0824/(2*pi*Fc*R)
Cb=0.9239/(2*pi*Fc*R)
Cc=2.6130/(2*pi*Fc*R)
Cd=0.3827/(2*pi*Fc*R)

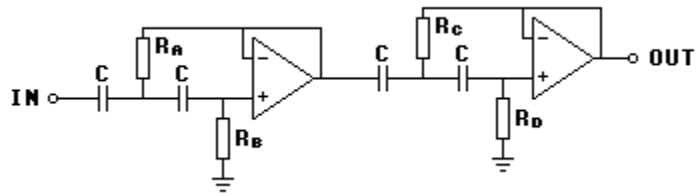
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Butterworth (4th order, 24 dB/octave, Highpass)



C=4.7n-10nF
Ra=0.9239/(2*pi*Fc*C)
Rb=1.0824/(2*pi*Fc*C)
Rc=0.3827/(2*pi*Fc*C)
Rd=2.6130/(2*pi*Fc*C)

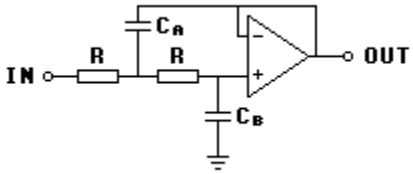
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Bessel
(2nd order, 12 dB/octave, Lowpass)



R=4.7k-10 kOhm
Ca=0.9076/(2*pi*Fc*R)
Cb=0.6809/(2*pi*Fc*R)

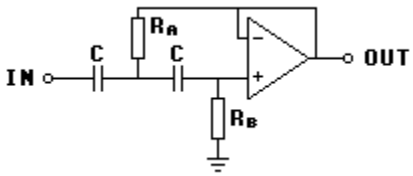
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Bessel
(2st order, 12 dB/octave, Highpass)



C=4.7n-10nF
Ra=1.1017/(2*pi*Fc*C)
Rb=1.4688/(2*pi*Fc*C)

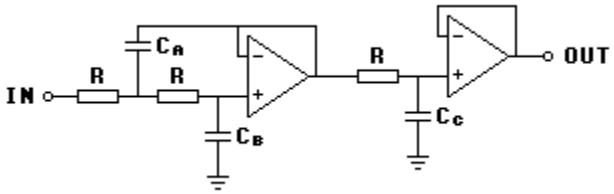
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Active Filter: Bessel 18dB Lowpass

Active Filter: Bessel
(3st order, 18 dB/octave, Lowpass)



R=4.7k-10 kOhm
Ca=0.9548/(2*pi*Fc*R)
Cb=0.4998/(2*pi*Fc*R)
Cc=0.7560/(2*pi*Fc*R)

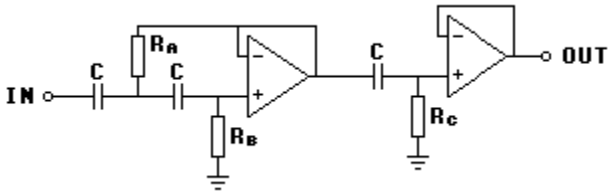
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Bessel
(3st order, 18 dB/octave, Highpass)



C=4.7n-10nF
Ra=1.0474/(2*pi*Fc*C)
Rb=2.0008/(2*pi*Fc*C)
Rc=1.3228/(2*pi*Fc*C)

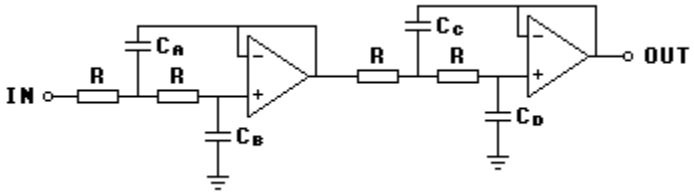
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Bessel
(4th order, 24 dB/octave, Lowpass)



R=4.7k-10 kOhm
Ca=0.7298/(2*pi*Fc*R)
Cb=0.6699/(2*pi*Fc*R)
Cc=1.0046/(2*pi*Fc*R)
Cd=0.3872/(2*pi*Fc*R)

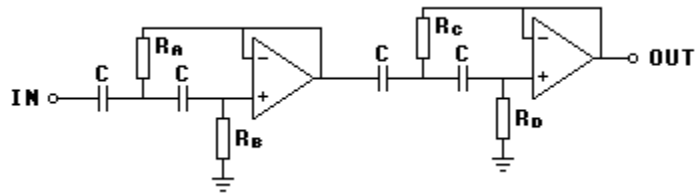
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Bessel
(4th order, 24 dB/octave, Highpass)



C=4.7n-10nF
Ra=1.3701/(2*pi*Fc*C)
Rb=1.4929/(2*pi*Fc*C)
Rc=0.9952/(2*pi*Fc*C)
Rd=2.5830/(2*pi*Fc*C)

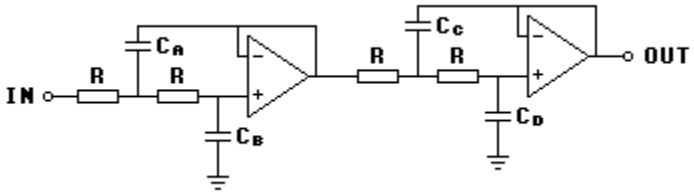
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Linkwitz
(4th order, 24 dB/octave, Lowpass)



R=4.7k-10 kOhm
Ca=Cc=2*Cb
Cb=Cd=1/(2*sqr(2)*pi*Fc*R)

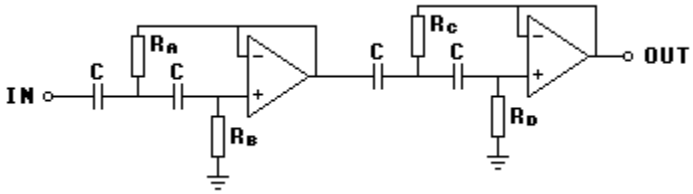
Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

NEW
NEW
NEW

Active Filter: Linkwitz
(4st order, 24 dB/octave, Highpass)



C=4.7n-10nF
Ra=Rc=1/(2*sqr(2)*pi*Fc*C)
Rb=Rd=2Ra

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

Definition: DTE & DCE

DTE

DTE is acronym for Data Terminal Equipment.

Examples of DTE is computers, printers & terminals.

DCE

DCE is acronym for Data Communication Equipment.

Examples of DCE is modems.

Wiring

Wiring a cable for DTE to DCE communication is easy. All wires goes straight from pin x to pin x.

But wiring a cable for DTE to DTE (nullmodem) or DCE to DCE requires that some wires are crossed. A signal should be wire from pin x to the opposite signal at the other end. With opposite signals I mean for example Transmit & Send.

Contributor: Joakim Ogren

Source:?

Please send any comments to Joakim Ogren.

WWW Links

NEW

NEW

Here are some links to good sites of technical information on the Internet.

I have a lot of pages I will add as soon as I get the time for it. They're currenly in my bookmarks file. Remember that I usually add links to pages covering a specific topic at bottom of the best suited HwB page.

Misc:

Name	Author	Comment
TheRef	F. Robert Falbo	Harddrives & controllers specifications.
Norm's Industrial Electronics NEW	Norman Dyrvik	Misc electronic links.
Circuit Cookbook	Dan Charrois	Various circuits.
PC Hardware Link Page	Dick Perron	Varoius Links and some own PC Hardware info.
Electrical Engineering Circuits Archive	Jerry Russell	Various circuits.
sandpile.org: 80x86 NEW	Christian Ludloff	Everything about 80x86 processors & motherbo
Hard Seek NEW	Davide Ferrari	Search for hardware manufacturers etc.
The Computer Information Centre NEW	Many	Contains very much about electronics/computer

FAQs:

Name	Author	Comment
alt.comp.hardware.homebuilt FAQ	Mark Sokos	Misc information about how to build your own th
sci.electronics FAQ: Repair: Pinouts FAQ	Filip M. Gieszczykiewicz	Misc pinouts for connectors.

If you have any more good links of interrest, please send me an e-mail at qtech@mailhost.net.

This is the URL for the WWW page:
http://theref.c3d.rl.af.mil/
Open this address in your WWW browser.

This the e-mail address:
falbof@rl.af.mil
Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.compusmart.ab.ca/ndyrvik/
Open this address in your WWW browser.

This the e-mail address:
ndyrvik@compusmart.ab.ca
Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.ee.ualberta.ca/~charro/cookbook/
Open this address in your WWW browser.

This the e-mail address:
charro@ee.ualberta.ca
Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.randomc.com/~dperr/pc_hdwe.htm
Open this address in your WWW browser.

This the e-mail address:

dperr@randomc.com

Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.ee.washington.edu/eeca/
Open this address in your WWW browser.

This the e-mail address:
pfloyd@u.washington.edu
Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.sandpile.org/80x86/
Open this address in your WWW browser.

This the e-mail address:
ludloff@sandpile.org
Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://notes.msoft.it/hw/default.cfm
Open this address in your WWW browser.

This the e-mail address:

ferrari@msoft.it

Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.compinfo.co.uk/index.htm
Open this address in your WWW browser.

This is the URL for the ftp:
ftp://ftp.netcom.com/pub/di/dibald/FAQS/achh.faq
Open this address in your WWW browser or FTP client.

This the e-mail address:

msokos1@gl.umbc.edu

Choose this address in your e-mail reader.

This is the URL for the WWW page:
http://www.paranoia.com/~filipg/HTML/REPAIR/F_Pinouts.html
Open this address in your WWW browser.

This the e-mail address:
filipg@paranoia.com
Choose this address in your e-mail reader.

Download Menu

The Hardware Book is availble in some other formats as well. Since these are converted from HTML the result may sometimes look a little bit strange. If there is some major visual errors or if a link doesn't work, feel free to send an e-mail. These versions is currently to be considered as beta. And btw, if you like to see HwB in some other format, let me know.

Visit HwB at Internet to download these versions.

HwB-News Menu

If you would like to be informed about what's happening with the Hardware Book, the HwB-News letter may be something for you. It will contain:

- Updates of The Hardware Book
- News concerning HwB.
- Info about HwB errors/typos.
- Related WWW Links

To subscribe to the HwB-News mailinglist send a mail with the text SUBSCRIBE in the body to hwb-news-request@www.blackdown.org

To unsubscribe to the HwB-News mailinglist send a mail with the text UNSUBSCRIBE in the body to hwb-news-request@www.blackdown.org

The mailing list is not a discussion mailinglist. It only contains mail from me, Joakim Ogren.

Note: It's a low traffic mailing list. Unsubscribe whenever you wan't, every mail contains unsubscribe instructions.

This the e-mail address:
hwb-news-request@www.blackdown.org
Choose this address in your e-mail reader.

Wanted

Please help me make this reference guide larger. I guess there is much more to add.
Don't hesitate to send some strange pinout, circuit or cable.
If you have a strange serial-port on your dish-washer, SEND it to me :-)
If it doesn't have one you could send me a circuit on how to add a serial-port to it. :-)
I'm especially searching for the following standards:

- NuBus (Apple Macintosh)
- SmallPCI
- SSFDC
- VMEbus
- VME64
- VXIbus
- SBX Bus
- STD Bus
- STEbus
- MCA (IBM)
- SBus
- MULTIBUS
- MULTIBUS II
- MTM-Bus
- TURBOchannel
- GIO
- Qbus
- PC/104
- AT96
- ISA96
- ECB
- SMP16
- ACCESS.bus
- FutureBus+
- SA1000
- JVC bus?
- SEGA Saturn A/V connector
- Playdia connectors
- Nec PC-FX connectors
- Neo Geo A/V connector
- Amstrad CPC6128 connectors

Other information of value:

- Filters

If you have any of the above listed please send me an e-mail at qtech@mailhost.net.

About Hardware Book

NEW

NEW

What about this? Your free reference guide to electronics.

The Hardware Book is a compilation of pinouts I've found from different sources. I've tried to have the same style for all pages. This makes it easier to find information for you. I'm not trying to sell anything.

It has been developed on my sparetime and is made availble to you for free. This also means that I can't guarantee that the presented information is correct. Use it on you own risk. I can't take the whole credit for HwB. I have since the first release recieved a great lot of mails with suggestions, questions and information. With the help of many contributors HwB has grown. Keep sending me mails...

Could it be even better? Perhaps if You help me. Please send any material you have that might be of interrest for this project. Send it to qtech@mailhost.net.

Visit the pages often. I will add things all the time. All new information will be marked NEW for about two weeks. And updated or changed information is marked NEW .

I would like to thank the following people:

Niklas Edmundsson	for helping me find some of the information in HwB and being a nice friend..
Karl Asha	for letting me use his web-server to store HwB.
Tomas Ogren	my brother, for comments and helping me with HwB.

This is what I feel like doing when nothing works ***:-)***

This the e-mail address:
qtech@mailhost.net
Choose this address in your e-mail reader.